Faculty Details proforma for DU Web-site

Title	Prof.	First Name	Mridula	Last Name	Gupta	Photograph
Designation		**Professor**				
Address		**Department of Electronic Science University of Delhi, South Campus New Delhi – 110 021**				
Phone No Office		**91-11-24115580**				
Residence		**91-11-28522365**				
Mobile		**9810868230**				
Email		**mridula_du@yahoo.com, mridula@south.du.ac.in**				
Web- Page						

Educational Qualifications		
Degree	Institution	Year
Ph.D.	**University of Delhi**	**1998**
M.Tech.	**University of Delhi**	**1988**
M.Sc. (Electronics)	**University of Delhi**	**1986**
B.Sc. (H) (Physics)	**University of Delhi**	**1984**
Any other qualification		

Career Profile

Organization	Designation	Duration	Role
Deptt. of Electronic Science, UDSC, INDIA	**Professor**	**10.08.2006 -till date**	**Teaching & Research**
Deptt. of Electronic Science, UDSC, INDIA	**Associate Professor/ Reader**	**10.08.1998-09.08.2006**	**Teaching & Research**
Deptt. of Electronic Science, UDSC, INDIA	**Lecturer**	**18.10.1989 - 09.08.1998 01.08.1988 - 30.04.1989 (Ad-hoc)**	**Teaching & Research**
C-DOT, Govt. of India	**Research Engineer**	**01.05.1989 - 17.10.1989**	**Design of Transreceiver**

Administrative Assignments

- **Appointment as the superintendent for the Post-Graduate Examinations of various departments under the South Delhi Campus w.e.f. March 25. 2015 to till date.**
- **Purchase Committee Member of W.U.S. Health Centre, University of Delhi, on March 23, 2015.**

- **Vice Chancellor Nominee as one of the expert member of the selection Committee for the interviews of the applicants under the stream Physical Sciences (Physics/Chemistry/Electronics), under the Faculty Training Program, University of Delhi, on February 25, 2015.**
- **Selection Committee Member for the Promotion of the Lecturer in the department of Physics and Electronics, Rajdhani College, University of Delhi, on February 25, 2015.**
- **Convener of the food Courts Committee, annual multifaceted academic and cultural festival (Antardhvani - 2015) organized by University of Delhi during February 20-22, 2015.**
- **Vice-Chancellor Nominee as an Expert for the Selection Committee for the post of Professor in Electronics and Communication Engineering , BPS Women University, Khanpur, Kalan, Sonepat on February 7, 2015.**
- **Purchase Committee Member of W.U.S. Health Centre, University of Delhi, on February 03, 2015.**
- **Vice-Chancellor Nominee of the selection committee for the post of Assistance Professor in the department of Computer Science, Shaheed Sukhdev College of Business Studies, University of Delhi, on November 28-29, 2014.**
- **Chairperson of the Selection Committee for the post of Assistance Professor in the department of Chemistry, Deshbandhu College, University of Delhi, on October 24-29, 2014.**
- **Member of the panel of paper Setters for M.Tech. (ICT) and M.Tech. Electronics and Communication Engineering, Bhagat Phool Singh Mahila Vishwavidyalaya, Khanpur Kalan (Sonepat), Haryana, India on September 9, 2014.**
- **Departmental Research Committee (DRC) member nomination by Vice Chancellor in the Department of Technology for the period of two years w.e.f. August 2, 2014.**
- **Expert Committee Member nomination by Chairman, UGC for the proposals received under Electronics and Communication Engineering Departments as per Special Assistance Programme (SAP) scheme on July 09, 2014.**
- **Expert Committee Member nomination by Chairman, UGC for preliminary evaluation of received online applications for Major Research Projects held on July 23, 2014.**
- **Expert Committee Member nomination by Chairman, UGC for evaluation and assessment of the proposals submitted by the College teachers for the purpose of availing travel grant assistance to attend the International Conferences abroad on September 25, 2014.**
- **Grievance Redressal Committee Member for two years of University of Delhi South Campus, w.e.f. December 3, 2014.**
- **Member of the panel, work related to objective type Question paper for Examination/test, Union Public Service Commission (UPSC) during December 15-16, 2014.**
- **Advisory Committee Member for Recent trends in Instrumentation and Electronics (RTIE -2015), Shaheed Rajguru College of Applied Science for Women, on January, 5-6, 2015.**
- **Technical Chair for Recent trends in Instrumentation and Electronics (RTIE -2015), Shaheed Rajguru College of Applied Science for Women, on January, 5-6, 2015.**
- **Expert Committee Member of UGC for the proposals received from University Departments (Electronics Science Engineering) as per Special Assistance Programme (SAP) scheme on January 14, 2015.**
- **Provost- Geetanjali Hostel South Campus, w.e.f. July 2014.**
- **Member & Treasure of Governing Body Deshbandhu College, Kalkaji, New Delhi, w.e.f. Sept. 2013.**
- **Member, General council of Netaji Subhas Institute of Technology (NSIT), Dwarka, w.e. f. Feb. 2014.**
- **Member of Governing body of Rajkumari Amrit Kaur College of Nursing w.e.f. April 2014.**
- **VC Nominee-DRC, IIC, UDSC, New Delhi-21, w.e.f. Jan. 2014.**
- **External expert of Board of Studies & Research in Department of Electronics & Communication Engineering of Guru Jambheshwar University of Science & Technology, Hisar, w.e.f. April 2014.**
- **External expert of Board of Studies & Research in Department of Electronics & Communication Engineering of Bhagat Phool Singh Mahila Vishvidyalaya, Sonipat, w.e.f. January 2014.**
- **Chairperson purchase committee-DOES UDSC New Delhi-21.**
- **Placement coordinator, Department of Electronic Science, University of Delhi, South Campus**
- **Coordinator B.Sc. (H) Electronics program**

Areas of Interest / Specialization

Modeling & characterization of submicron and deep submicron field effect devices. This includes the Si MOSFET,

Tunnel FET, MESFET, GaAs MESFET and GaAs/InP HEMT

Subjects Taught

27 years teaching experience of M.Sc. (Electronics), M.Sc. (Informatics) and M.Tech. (Microwave Electronics) classes.
Modern Communication Systems, Analog & Digital Circuit Design, Control Systems, Communication Theory

Research Guidance

List against each head (If applicable)

1. *Supervision of awarded Doctoral Thesis* - ***19***
2. *Supervision of Doctoral Thesis, under progress* - ***07***
3. *Supervision of awarded M.Phil dissertations* - ***Nil***
4. *Supervision of M.Phil dissertations, under progress* - ***Nil***

S.No.	Name	Year	Title of the Thesis
1.	Gupta, Ritesh	2003	Modeling, Characterization and Optimization of InAlAs/InGaAs Heterojunction, InP based High Electron Mobility Transistor (HEMT) For Microwave and Millimeter Wave Frequency Applications
2.	Singh, Adarsh	2004	Analytical Modeling, Analysis and Characterization of GaN MESFET for Optoelectronic Applications
3.	Sehgal, Amit	2007	Poly-Crystalline Silicon Thin Film Transistors: Modeling, Simulation and Characterization
4.	Mangla, Tina	2007	Modeling and Simulation Characterization of Nano Scale MOSFETs with Quantum Mechanical Effects and Gate Stack Engineering for ULSI
5.	Goel, Kirti	2007	Two Dimensional Analytical Modeling and Simulation of Non-Uniformly Doped Dual Martial Gate(DMG) and Triple Material Gate (TMG) MOSFET Structures
6.	Aggarwal, Sandeep	2008	Correlation & Enhancement of Circuit Parameters with Device Parameters of Different Metal-Insulator Geometric Single/ Double/Dual Gate 4H-SiC MESFET
7.	Kabra, Sneha	2008	Modeling Simulation and Characterization of GaN MESFET
8.	Parvesh	2008	Polarization dependent analysis and characterization of AlGaN/GaN HEMT
9.	Chaujar, Rishu	2008	Analytical modeling and simulation of gate electrode workfunction and dielectric engineered recessed channel MOSFET in Sub-100nm Regime
10.	Kumar, Sona P.	2010	Analysis , Modeling and Simulation of AlGaN/GaN Modular Doped Field Effect Transistor
11.	Sharma, Rupendra	2010	Two Dimensional Analytical Modeling and Simulation of Gate Misalignment Effect in Fully Depleted Double Gate MOSFET
12.	Aggarwal, Ruchika	2011	Modeling, Characterization and Simulation of AlGaN/GaN Metal Insulator Semiconductor Heterostructure Field Effect Transistor(MISHFET) for High Power Microwave Applications
13.	Rathi, Servin	2012	Modeling, Simulation & Characterization of Modified Different Gate Geometric Double Gate High Electron Mobility Transistor for High Power and High Frequency Applications with Two Separate/Common Gate

			Control
14.	Malik, Priyanka	2013	Analytical modeling and simulation of advanced MOSFET structures in sub-100nm regime
15.	Ghosh, Pujarini	2013	Capacitive Modeling Simulation and Characterization of Surrounded/Cylindrical Gate MOSFET (SGT/CGT) for High Frequency Applications
16.	Gautam, Rajni	2014	Analytical modeling and simulation of cylindrical gate all around MOSFET-reliability and sensor applications
17.	Bhattacharya, Monika	2014	Modeling, Simulation and Characterization of Noise in InAlAs/InGaAs Tied-geometry Double-gate High Electron Mobility Transistor for Millimeter-wave Applications
18.	Kumari, Vandana	2014	Impact of Dielectric Pocket on Different Gate Geometry MOSFET Architectures for Improved Analog and Digital Performance: Modeling and Simulation
19.	Narang, Rakhi	2014	Analytical Modeling and Simulation of Multiple Gate Geometry Tunneling Field Effect Transistors for Low Power Logic Circuit Design and Biosensing Applications
20.	Pratap, Yogesh	In progress	Modelling and Characterization of all around Gate Nano-Scale MOSFETs
21.	Verma, Jay Hind Kumar	In progress (16th April 2013)	Noise Analysis and Modeling of Cylindrical/surrounding gate MOSFET
22.	Kadam, Upasana	In progress (16th April 2013)	Steep sub-threshold devices for energy efficient circuits: Modeling and simulation
23.	Ajay	In progress (27th July 2013)	Analytical Modeling and Simulation study of BioFETs for label free electrical detection of biomolecules
24.	Kumar, Sachin	In progress (27th July 2013)	Design and Development of Simulation Framework for microelectronic devices
25.	Kumar, Manoj	In progress (6th May 2014)	Analytical modeling, simulation and characterization of schottky barrier (SB) gate all around (GAA) MOSFET structures for low power applications
26.	Chander, Subhash	In progress (24th April 2014)	Simulation, Modeling and Characterization of MMIC (Monolithic Microwave Integrated Circuit) Comopents

Publications Profile

List against each head(If applicable) (as Illustrated with examples)

1. *Books/Monographs (Authored/Edited)*
2. *Research papers published in Refereed/Peer Reviewed Journals*
3.
   a) *Research papers published in Academic Journals other than Refereed/Peer Reviewed Journals*
   b) *Research papers published in Refereed/Peer Reviewed Conferences*
   c) *Research papers Published in Conferences/Seminar other than Refereed/Peer Reviewed Conferences*
4. *Other publications (Edited works, Book reviews, Festschrift volumes, etc.)*

Research papers published in Refereed/Peer Reviewed journal (August 2014- July 2015)

1. Kumar Manoj, Haldar S., Gupta Mridula, Gupta R. S. 2014 'Impact of Gate Material Engineering(GME) on Analog/RF Performance of Nanowire Schottky-Barrier Gate All Around (GAA) MOSFET for Low Power Wireless applications: 3D T-CAD Simulation' Micro Electronics Journal, Vol. 45, no. 11, pp. 1508–1514, 2014. (Nov).
2. Narang Rakhi, Saxena Manoj and Gupta Mridula. 2015 'Comparative Analysis of Dielectric Modulated FET and TFET based Biosensor" Rakhi Narang, Manoj Saxena and Mridula Gupta, IEEE Trans. On Nanotechnology, Vol. PP, no.99, 2015. (May)
3. Kumari Vandana, Saxena Manoj and Gupta Mridula. 2015 'Modeling and Simulation of Double Gate Junctionless Transistor Considering Fringing Field Effects" Vandana Kumari, Neel Modi, Manoj Saxena and Mridula Gupta, Solid State Electronics, Vol. 107, pp.20-29, 2015. (May)
4. Kumari Vandana, Saxena Manoj and Gupta Mridula. 2015 'Theoretical Investigation of Dual Material Junctionless Double Gate Transistor for Analog and Digital Performance' IEEE Trans. On Electron Devices, Vol. 67, no.7 pp.2098-2105, 2015.(July).
5. Ajay, Narang Rakhi, Saxena Manoj and Gupta Mridula. 2015 'Drain Current Model of a Four-Gate Dielectric Modulated MOSFET for Application as a Biosensor' IEEE Trans. On Electron Devices, Accepted for publication, 2015.(June).
6. Upasana, Narang Rakhi, Saxena Manoj and Gupta Mridula. 2015 'Linearity and analog performance realization of energy efficient TFET based architectures: An Optimization for RFIC Design', IETE Technical Review, pp. 1-6, 18, June, 2015.
7. Pratap Yogesh, Haldar S., Gupta R. S. and Gupta Mridula 2015"Localised Charge Dependent Threshold Voltage Analysis of Gate Material Engineered Junctionless Nanaowire Transistor," IEEE Transactions on Electron Device, Accepted for publication, 2015.

International/National Conferences: (AUGUST 2014- July 2015)

8. Sachin, Kumari Vandana, Saxena Manoj and Gupta Mridula. 2014 'TCAD Assessment of Nanoscale Double Gate RingFET (DG-RingFET) Architecture: Analog and Linearity Performance Investigation for RFIC Design" Sachin Kumar, Vandana Kumari, Manoj Saxena and Mridula Gupta, International conference on Nanotechnology (NANOCON, Pune, India), October 14-15, 2014.
9. Kumari Vandana, Saxena Manoj and Gupta Mridula. 2014 'Modeling and Simulation of Nanoscale Lateral Gaussian Doped Channel Asymmetric Double Gate MOSFET" Vandana Kumari, Manoj Saxena and Mridula Gupta, International conference on Nanotechnology (NANOCON, Pune, India), October 14-15, 2014.
10. Kumari Vandana, Saxena Manoj and Gupta Mridula. 2014 'Charge Based Modeling of channel Material Engineered P-type Double Gate MOSFET" Vandana Kumari, Aravindin Ilango, Manoj Saxena and Mridula Gupta, 2nd **International Conference on Emerging Electronics** (ICEE, Bangalore, India) December 4-6, 2014.
11. Kumari Vandana, Saxena Manoj and Gupta Mridula. 2014 'Modeling and Simulation of Nanoscale III-V based Tri-Gate Stack MOSFET on Nothing for Improved Analog and Digital Applications" International conference of recent advances in Nanoscience and Nanotechnology (ICRANN, New Delhi, India) December 15-16, 2014.
12. Upasana, Narang Rakhi, Saxena Manoj and Gupta Mridula. 2014 'Drain Current Model for Hetero-Dielectric based TFET Architectures: Accumulation to Inversion Mode Analysis", International conference on Nanotechnology (NANOCON, Pune, India), October 14-15, 2014.
13. Ajay, Narang Rakhi, Saxena Manoj and Gupta Mridula. 2014 'pH sensing Characteristics of Silicon on Insulator (SOI) Junctionless (JL) ISFET" International conference on Nanotechnology (NANOCON, Pune, India), October 14-15, 2014.
14. Narang Rakhi, Saxena Manoj and Gupta Mridula. 2014 'Numerical Analysis of Variability effects in Nanogap Embedded Dielectric Modulated Field Effect Transistor", International conference on Nanotechnology (NANOCON, Pune, India), October 14-15, 2014.
15. Upasana, Narang Rakhi, Saxena Manoj and Gupta Mridula. 2014 'Dielectric Pocket Tunnel FET: A Reliable Alternative", International conference of recent advances in Nanoscience and Nanotechnology (ICRANN, New Delhi, India) December 15-16, 2014.
16. Narang Rakhi, Saxena Manoj and Gupta Mridula. 2015 'Polarity and Ambipolarity Controllable (PAC) Tunnel Field Effect Transistor' 11th IEEE Conference on Electron Devices and Solid State Circuits, Singapore, 1st-4th June 2015.

17. Narang Rakhi, Saxena Manoj and Gupta Mridula. 2015 'Impact of Dry and Watery Environment on the Sensitivity of Split Gate Metal Oxide Field Effect Transistor for Biosensing Application' 11th IEEE Conference on Electron Devices and Solid State Circuits, Singapore, 1st-4th June 2015.
18. Upasana, Narang Rakhi, Saxena Manoj and Gupta Mridula. 2015 "Influence of dielectric pocket on electrical characteristics of tunnel field effect transistor a study to optimize the device efficiency' 11th IEEE Conference on Electron Devices and Solid State Circuits, Singapore, 1st-4th June 2015.
19. Verma J. H. K., Haldar Subhasis, Gupta R.S. and Gupta Mridula. 2014 "Impact of Inner Charge Control Gate on CSG MOSFET for Improved Electrostatic Integrity and RF Performance", Jay Hind Kumar Verma, Subhasis Haldar, R.S. Gupta and Mridula Gupta 3rd International Conference on Nanotechnology (NANOCON04), 14th-15th October-2014, Pune India
20. Pratap Yogesh, Haldar Subhasis, Gupta R.S. and Gupta Mridula. 2014. "Damage Immune III-V Compound Material based Vacuum Junctionless Nanowire Transistor (VAC-JNT) for Improved Electrostatic Control and Hot Carrier Reliability," 3rd International Conference on Nanotechnology (NANOCON04), 14th-15th October-2014, Pune, India.
21. Verma J. H. K., Haldar Subhasis, Gupta R.S. and Gupta Mridula. 2014 'Material Engineering in Cylindrical Surrounding Double Gate (CSDG) MOSFETs for Enhance Electrostatic Integrity and RF Performance" (ICEE), 3rd-6th December-2014, Bangalore India.

Conference Organization/ Presentations (in the last three years)

List against each head(If applicable)

1. *Organization of a Conference*

- ***Mini Colloquia on "Compact Modelling Techniques for Nanoscale Devices and Circuit Analysis*** organized by **IEEE EDS Delhi Chapter** at University of Delhi South Campus, New Delhi, India on March 13, 2015
- ***First National Conference on Recent Development in Electronics (NCRDE-2013)*** by **IEEE EDS Delhi Chapter** at University of Delhi South Campus, New Delhi, India on January 18-20, 2013
- ***Mini-colloquia on Compact Modelling Techniques for Nanoscale Devices and Circuit Analysis*** organized by **IEEE EDS Delhi Chapter** at University of Delhi South Campus, New Delhi, India on March 14-15, 2012
- ***Science Academies Lecture Workshop on Frontiers in Science & Engineering Opportunities for Graduates*** which was jointly Organized by Deen Dayal Upadhyaya College, University of Delhi, New Delhi and IEEE EDS Delhi Chapter, New Delhi, February 17-18, 2012.

2. *Participation as Paper/Poster Presenter*

- **IEEE Conference on Electron Devices and Solid State Circuits 2015**, Singapore, 1st-4th June 2015.
- IEEE ***INDICON 2013 (Innovations in Social and Humanitarian Engineering),*** IIT Bombay, Powai, Mumbai, India, Dec 13th -15th, 2013.
- ***ICEE 2012 (International Conference on Emerging Electronics)***, IIT Bombay, Powai, Mumbai, India, Dec 15-17, 2012
- ***IEEE INDICON 2012 (Innovations in Social and Humanitarian Engineering),*** Kochi, Kerala, India, Dec 7-9, 2012.
- ***International conference on VLSI, MEMS & NEMS. (VMN 2012),*** Amity School of Engineering & Technology, Amity University, Uttar Pradesh, India, January 24-25, 2012.
- ***VLSI Design and Test symposium (VDAT-2011***). Pune, India, July 7- 9, 2011.
- ***IEEE TENCON 2011,*** Bali, Indonesia, Nov 21-24, 2011.

Research Projects (Major Grants/Research Collaboration)

1. **DST sponsored project:** Analytical Modeling and Simulation for sub-100nm Advance Tunnel FET architectures for RF/Microwave and Biosensing Applications. (In Progress)

2. **DU sponsored project:** Device and Circuit Level Performance Investigation of Junctionless Field Effect Transistors and its Applications. (In Progress)

Awards and Distinctions

1. Received IEEE EDS best Chapter of the year award-2013
2. Received **University Gold Medal** in 1986 for being the **best candidate** in the M.Sc. (Electronics) examination.
3. **Stood first** in the order of merit in M.Tech. (Microwave Electronics) examination in 1988.
4. Awarded **Nehru Centenary Common Wealth Fellowship (UK)** for three years in 1990.

Association With Professional Bodies

1. *Editing*
2. *Reviewing*
   - IEEE Transactions on Electron Devices
   - IEEE Electron Device Letters
   - Microelectronics Reliability
   - Applied Physics letters
   - International Journal of Numerical Modeling (IJNM)
   - Journal of Semiconductor Technology and Science (JSTS)
   - IET-Circuit Device and Systems (CDS)
3. *Advisory*
4. *Committees and Boards*
5. *Memberships*
   - **Senior Member IEEE**
   - **Fellow** – The Institution of Electronics and Telecommunication Engineers.
   - **Life Member** – Semiconductor Society of India.
6. *Office Bearer*
   - **Life Member & Secretary** – Society for Microelectronics and VLSI, India.
   - **Chairman –** IEEE-EDS Delhi Chapter

Other Activities

Have been actively engaged in various activities of the Department (July 2014-June 2015)

- Lecture Series
  - ***One day interactive session on Silvaco Full flow design tools for all semiconductor Technologies at Department of electronics Science, University of Delhi, New Delhi, India, April 13, 2015, by Dr. P. K. Saxena India Regional Head, Silvaco Singapore Pte. Ltd.***