Appendix A

The main objective of the project is to develop two dimensional analytical model of drain current for III-V based material Ring FET which can be used further for assessing the analog and linearity performance of the device. For RF performance assessment, various electrical parameters such as unity gain cut-off frequency (f_T), maximum oscillation frequency (F_{max}), intrinsic delay, etc. shall be extracted through extensive device simulation. The Circuit performance of the Ring FET shall also be studied through RingFET based inverter logic gates, flip-flop and SRAM. Application of Ring FET as a sensor shall be explored in the last phase of the project. Using the analytical model and through exhaustive device simulations, an optimized device design shall be proposed having enhancement in the cross sensitivity towards sensing material.

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Appendix B

Report of the work done (Phase wise)

Phase – I

Appointment of manpower. Introduction of the research problem to the research scholar and complete literature survey of the proposed work.

Phase – II

Two dimensional analytical model for drain current shall be developed for III-V Ring FET drain current expression shall be used to derive the trans-conductance (g_m), and its higher order derivatives useful for assessing the linearity performance. The analytical expression of trans-conductance (g_m) and drain-conductance (g_d) shall be useful for deriving analytical expression of trans-conductance generation efficiency (g_m/I_{ds}), intrinsic gain (g_m/g_d) and on-resistance (R_{on}).

Brief Review

"Two dimensional (in cylindrical coordinates), analytical drain current model of a nanoscale RingFET architecture has been developed and compared with simulated data using ATLAS 3D device simulator. Major short-channel effects, such as channel length modulation, velocity scattering, and drain-induced barrier lowering, are taken under consideration while developing the model. A bandgap narrowing model has been employed to investigate the impact of higher channel doping. The modeled results of the surface potential, electric field, threshold voltage (V_{th}), subthreshold slope, drain current and trans-conductance have been verified by comparing with those of the ATLAS 3-D device simulation. The influence of the drain radius and position of the source/drain regions on the electrical characteristics of the device has also been demonstrated"

"The impact of channel material engineering (i.e. III-V compound semiconductor) and gate oxide engineering on the RingFET architecture has been investigated. The investigation involves the study of various electrical parameters like drive current (I_{ds}-V_{gs}), threshold voltage (V_{th}), Sub-threshold Slope (SS), Drain Induced Barrier Lowering (DIBL), $I_{ON/OFF}$' and transconductance generation efficiency (g_m/I_{ds}), under different device specifications. Apart from these, reliability issues the excessive gate leakage current has also been addressed."

"A novel device design i.e. Skin Deep Insulated Extension-RingFET (i.e. SDIE-RingFET) has been proposed that incorporates the effects of dielectric pocket in RingFET architecture. Various analog performance matrices like I_{ON}/I_{OFF}, V_{th} roll off, Sub-threshold slope (SS), Device efficiency (g_m/I_{ds}), conduction band energy (CBE) and electron temperature have been studied to investigate the impact of Skin Deep Insulated Extension (SDIE) on RingFET architecture. Insulated extension enhances the immunity of the device against Short Channel Effects by reducing IOFF and providing a higher ION/IOFF ratio apart from improved threshold voltage roll-off. In addition, SDIE also prevents dopant diffusion from source/drain to bulk, thereby alleviating the bulk punch-through effect and hence DIBL."

In the completion of Phase-II, the following work was published.

1. Sachin Kumar, Vandana Kumari, Sanjeev Singh, Manoj Saxena and Mridula Gupta, "Nanoscale-RingFET: An Analytical drain Current Model including SCE's" **IEEE Transactions on Electron Devices**, Vol.62(12), pp. 3965 – 3972 Nov. 2015. ISSN No. 0018-9383, DOI: 10.1109/TED.2015.2493578, Impact Factor: 2.512.

2. Sachin Kumar, Vandana Kumari, Sanjeev Singh, Manoj Saxena and Mridula Gupta, "Reconnoiter the leavening of skin-deep insulated extension on analog performance of RingFET (SDIE-RingFET)" International Journal of Electronics and Communications (AEÜ), Vol.83, pp. 67-72, Nov. 2018, ISSN No. 1434-8411, DOI: https://doi.org/10.1016/j.aeue.2017.07.038, Impact Factor: 1.147.
3. Sachin Kumar, Vandana Kumari, Manoj Saxena and Mridula Gupta, "Investigation of III-V Compound Semiconductor Materials on Analog performance of Nanoscale RingFET" **Annual IEEE India Conference-INDICON**-2015, 17th- 20th Dec. 2015, Delhi, **Electronic ISSN:** 2325-9418, DOI: 10.1109/INDICON.2015.7443776.

Phase – III

For RF performance assessment, various electrical parameters such as unity gain cut-off frequency (f_T), maximum oscillation frequency (F_{max}), intrinsic delay, etc. shall be extracted through extensive device simulation. To assess the linearity performance of the concerned device, simple and reliable metrics (VIP_2, VIP_3, IIP3, IMD3 etc.) shall be evaluated.

Brief Review

"TCAD based investigation of RingFET architecture has been carried for high frequency applications. ATLAS TCAD device simulation software has been used to exploits the RingFET performance and are also compared with the equivalent bulk MOSFET. Parameters such as: cut-off frequency, max. transducer power gain, Stern Stability factor, Unilateral power gain, scattering parameters and parasitic capacitance (i.e. C_{gs} and C_{gd}) are evaluated. Maximum cut-off frequency of 3.7 THz has been achieved with RingFET (having drain outside) architecture at 32nm channel length. With the reduction in substrate doping, gate work-function and enhancement in gate voltage superior cut-off frequency can be achieved. Due to asymmetric nature of RingFET architecture, lower cut-off frequency is observed in drain inside RingFET (i.e. 3.4 THz) compared to drain outside. Also, the change in gate to source capacitance C_{gs} with substrate doping is higher in comparison to gate to drain capacitance C_{gd} in RingFET."

"Impact of Double Gate on RingFET (DG-RingFET) architecture has been investigated for better gate control and suppressed Short Channel Effects (SCEs) using ATLAS 3D device simulator. The analog performance metrics explored are drain current (I_{ds}-V_{gs}), trans-conductance (g_m), device efficiency (g_m/I_{ds}), and early voltage (V_{ea}). In addition to this linearity behaviour of DG-RingFET has been investigated in terms of third-order voltage intercept point (VIP_3), third-order current intercept point (IIP_3), third-order inter modulation distortion (IMD_3) and results are also compared with the single gate architecture."

"The two-dimensional analytical model for DG-RingFET architecture has also been developed in this paper using parabolic approach. Moreover, the impact of technology variations like drain radii and position of drain, i.e. inside or outside the channel ring on the performance of DG-RingFET architecture has also been assessed. Impact of high-K gate dielectric on the performance of DG-RingFET has also been observed which results in superior Ion along with deterioration in leakage current "

- **In the completion of Phase-III, the following work was published.**

1. Sachin Kumar, Vandana Kumari, Manoj Saxena, Mridula Gupta, "Hot Carrier Reliability and linearity Performance Investigation of Nanoscale RinFET for RFIC Design", International Conference on Microwave, Antenna, Propagation and Remote sensing (ICMARS 2013), 11th – 14th December pp. 40-44, Jodhpur, India.

2. Vandana Kumari, Sanjeev Singh, Manoj Saxena and Mridula Gupta "RingFET Architecture for High Frequency Applications: TCAD based Assessment" ***Communicated in EDKcon-2018.***
3. Sachin Kumar, Vandana Kumari, Sanjeev Singh, Manoj Saxena and Mridula Gupta, "Sub-threshold Drain Current model of Double Gate RingFET (DG-RingFET) Architecture: An Analog and Linearity Performance Investigation for RFIC Design" **IETE Technical Review**, pp. 1-10, Jan 2017. ISSN No. 0974-5971. Impact Factor: 1.330. DOI: http://dx.doi.org/10.1080/02564602.2016.1270174
4. Sachin Kumar, Vandana Kumari, Sanjeev Singh, Manoj Saxena and Mridula Gupta, "Impact of High-K Gate Dielectric on Double Gate RingFET (HK-DGRingFET) Architecture", National Conference on Recent Developments in Electronics (NCRDE-2017), pp.177-180, February 17-18, 2017, Delhi, India.

Phase – IV

The Circuit performance of the Ring FET (i.e. Ring FET based inverter logic gates, flip-flop and SRAM) shall be studied in this phase through exhaustive device and circuit simulation and also compared with the other conventional device architectures based circuits to assess its (i.e. Ring FET) usability for high speed low power digital application.

Brief Review

"The impact of gate material engineering on the performance of RingFET architecture i.e. Dual Material Gate RingFET (DMG-RingFET) has been investigated using ATLAS 3D device simulation. A fair comparison has also been drawn between the performance of DMG-RingFET and SMG RingFET device architectures. The impact of high-k gate dielectric on the performance of DMG RingFET has also been presented. Various important analog and digital performance metrics such as drain current (I_{ds}), transconductance (g_m), transconductance generation efficiency (g_m/I_{ds}), early voltage (V_{ea}). Apart from these, to investigate digital performance, DMG-RingFET based NMOS-inverter has been simulated and also compared with conventional RingFET based inverter. Output voltage of inverter and inverter gain has been discussed in detail to study noise margin of the device. In addition to this, investigation of DMG-RingFET as an inverter has been performed to demonstrate the reliability of DMG-RingFET architecture for digital circuit application."

In the completion of Phase-IV, the following work was published.

1. Sachin Kumar, V. Kumari, M. Saxena, and M. Gupta, "TCAD Assessment of Dual Material Gate Nanoscale RingFET (DMG-RingFET) for Analog and Digital Applications" International Conference on Devices Circuit and System-2014, pp. 1-5, Coimbatore, Tamilnadu, India, 2014, DOI: 10.1109/ICDCSyst.2014.6926181 ISBN- 978-1-4799-1356-5

Phase – V

The application of Ring FET as a sensor shall be studied in the last phase of the project and enhancement in the cross sensitivity towards sensing material shall be explored using different channel material. An optimized device design shall be developed through device simulation and physics based analytical model.

Brief Review

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In order the check the sensitivity of RingFET architecture, behavior of RingFET as gas sensor has been examined. When the device has been exposed to gas, partial pressure of the gas on to the gate results in change in work-function of the catalytic gate thereby leading to change in I_{off}, I_{on} and threshold voltage of the device. Compared to equivalent bulk MOSFET, bulk RingFET shows higher sensitivity (i.e. change in Ioff when device is exposed under gas molecule) towards gas molecules. Also, the device is highly sensitive against gas molecules at lower drain bias i.e. V_{ds}=0.1V. Different III-V compound semiconductors (i.e. GAN, InGAN, and GaAs) has also been used to check the sensitivity of the device. Compared to silicon, GaAs has higher carrier mobility, however the change in I_{off} with gate workfunction (due to exposure of gas molecules) is lower in GaAs RingFET. Compared to silicon, the sensitivity of RingFET having GaN and InGaN has higher sensitivity towards gas molecules. It has also been observed that, reduction in channel doping results in deterioration in sensitivity of the bulk RingFET. Different gate dielectrics has also been used to investigate the sensitivity of the bulk RingFET. Compared to SiO2 based GaN-RingFET, HfO2 gate dielectric shows higher sensitivity i.e. change in I_{off} with gas molecules. At higher channel length, sensitivity of device improves due to higher exposure area of the device. However, by changing the source drain length slight modifications in the sensitivity has been observed.

The work done in this phase is yet to be communicated.

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Appendix C

ACHIEVEMENTS FROM THE PROJECT

- Analytical Model for RingFET architecture has been developed which is valid for shorter channel lengths.

- By employing III-V semiconductor, improvement in I_{on}, I_{on}/I_{off} ratio and sub-threshold slope has been observed with slightly higher gate leakage current. Roll-off with channel length is also lower in GaAs based RingFET.

- A novel device design i.e. Skin Deep Insulated Extension-RingFET (i.e. SDIE-RingFET) has been proposed that incorporates the effects of dielectric pocket in RingFET architecture. The implanted insulated extension prevents the flow of leakage current from drain to source resulting in improvement of I_{ON}/I_{OFF} ratio, TGF (g_m/I_d).

- Maximum cut-off frequency of 3.7 THz has been achieved with RingFET (having drain outside) architecture at 32nm channel length which is superior than equivalent bulk MOSFET. Due to asymmetric nature of RingFET architecture, lower cut-off frequency is observed in drain inside RingFET (i.e. 3.4 THz) compared to drain outside.

- Impact of Double Gate on RingFET (DG-RingFET) architecture has been investigated for better gate control and suppressed Short Channel Effects (SCEs). Apart from superior DC performance parameters (i.e. lower sub-threshold slope, higher I_{on}/I_{off} ratio and lower DIBL), DG-RingFET also shows better linearity behavior i.e. lower higher order harmonics compared to bulk RingFET.

- Full drain current model for DG-RingFET has also been developed and the impact of high-k gate dielectric on the performance of DG-RingFET has been investigated. high-K DG-RingFET results in superior I_{on} along with deterioration in leakage current with lower threshold voltage roll-off with channel length.

- The gate material engineering technique has also been used which boost the performance by suppressing the SCEs in terms of lower DIBL and higher I_{on}/I_{off} ratio. Inverter based on DMG-RingFET also provide superior noise margin and better reliability compared to RingFET architecture.

- Sensitivity of the RingFET architecture against gas molecules has also been studied by changing the work-function of the catalytic gate. Compared to bulk MOSFET, higher sensitivity against gas molecules has been achieved from bulk RingFET. Among various semiconductors (i.e. silicon, GaAs, InGaN and GaN) GaN based RingFET has superior sensitivity.

- An open platform modeling-based device simulation module has been developed which can be used by students (under Graduate, Post Graduate and PhD students of Engineering or Applied Science streams) to have a hands-on experience on VLSI. This work focuses on development of GUI based platform. In addition to this the developed platform has web-based interface which gives the user more friendly and versatile environment. The platform has been designed using web2.0 technologies. The frontend is powered by HTML5/CSS3 and JavaScript, while the backend – the core processing and analytics unit – is implemented in PYTHON. Since it is open source license, thus students can easily access this tool in comparison to the existing commercial license tools.

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Appendix D

As MOSFET gate length is scaled down to sub-100 nm, the leakage current drastically increases. But scaling poses many challenges as it enters into the nanometer regime. To overpower these challenges, new materials and novel device architectures are needed in order to guarantee the ultimate scaling in device dimensions and maintain the performance gain expected from the scaling. Incorporating novel technological solution to oxide and gate material, the electric field and the electrostatics in the channel can be controlled in a more efficient way.

RingFET is one of the non classical bulk MOSFET architecture offering superior CMOS device features with higher speed, higher density and reduced second order effects for submicron VLSI applications. Recent studies invigorated interest in RingFET device because of its potentially superior scalability relative to bulk silicon CMOS devices. Also, various new structures with different engineering concepts have been reported to reduce the SCEs on Bulk MOSFET platform. Among them Gate Material Engineering, Channel Material Engineering, Double Gate Engineering technology are very popular for enhancing the gate controllability, increasing the carrier mobility and reduction of gate leakage current. Apart from immunity against short channel effects, reliability is a major concern for nanoscale devices. The scaling trends in MOSFETs, operating conditions, process induced damage and radiation induced damage give rise to serious device and circuit reliability issues. All these degradation mechanisms lead to generation of localized interface trap charges at the semiconductor and oxide interface of the MOSFET which lead to device performance degradation in terms of shift in threshold voltage, drain current and transconductance. International Technology Roadmap for Semiconductors mentions reliability as one of the "Design Technology Challenges" and calls attention to "Design for Reliability." In order to increase the overall design efficiency, it is important to understand MOSFET-level degradation by developing analytical compact models. Then to overcome these degradations, new device architectures/techniques shall be explored, which are self sufficient in preventing these malefic effects. In this dissertation, various novel device engineering techniques has been investigated over RingFET architecture by developing analytical model and extensive device simulation.

In this project, we have investigated

1. Suitability of RingFET architecture for analog circuit applications by developing an analytical model using Evanescent Mode Analysis approach. Investigation of device geometry on various analog performance matrices has also been performed. In addition to this reliability assessment of the device has also been done under the impact of interface trap charges.
2. New device architecture i.e. Skin Deep insulated Extension Ring FET has also been proposed to overcome the punchthrough effect.
3. To further enhance the device performance a new architecture has also been reported i.e. by using the Gate electrode/oxide material engineering (namely SMG-RingFET, DMG-

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RingFET,DMG-RingFET). DMG-RingFET based inverter has also higher noise margin as compared to bulk RingFET.

4. Double Gate RingFET has also been proposed having higher gate controllability compared to bulk RingFET. Linearity performance of the Double Gate RingFET is also superior than bulk RingFET due to lower higher order harmonics.
5. Since the detection of gas molecules has also been immensely important now a days. Thus, the suitability of bulk RingFET as gas sensor has been analysed and compared with equivalent bulk MOSFET.
6. An open platform modeling-based device simulation module has been developed which can be used by students (under Graduate, Post Graduate and PhD students of Engineering or Applied Science streams) to have a hands-on experience on VLSI. This work focuses on development of GUI based platform. In addition to this the developed platform has web-based interface which gives the user more friendly and versatile environment. The platform has been designed using web2.0 technologies. The frontend is powered by HTML5/CSS3 and JavaScript, while the backend – the core processing and analytics unit – is implemented in PYTHON. Since it is open source license, thus students can easily access this tool in comparison to the existing commercial license tools.

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Appendix E

Summary of the Finding

1. Two dimensional (in cylindrical coordinates), analytical drain current model of a nanoscale RingFET architecture has been developed. A bandgap narrowing model has been employed to investigate the impact of higher channel doping. The modeled results of the surface potential, electric field, threshold voltage (V_{th}), subthreshold slope, drain current and trans-conductance have been verified by comparing with those of the ATLAS 3-D device simulation.

2. The impact of channel material engineering (i.e. III-V compound semiconductor) and gate oxide engineering on the RingFET architecture has been investigated which involves the calculation of current (I_{ds}-V_{gs}), threshold voltage (V_{th}), Sub-threshold Slope (SS), Drain Induced Barrier Lowering (DIBL), $I_{ON/OFF}$' and transconductance generation efficiency (g_m/I_{ds}). Reliability of the device in terms of gate leakage current has also been investigated under different operating conditions and interface instability.

3. To curb the short coming of bulk RingFET, Skin Deep Insulated Extension-RingFET (i.e. SDIE-RingFET) has been proposed that incorporates the effects of dielectric pocket in RingFET architecture. Performance metrics which governs the digital performance of the device are mainly investigated like I_{ON}/I_{OFF}, V_{th} roll off, Sub-threshold slope (SS), Device efficiency (g_m/I_{ds}), conduction band energy (CBE) and electron temperature. SDIE-RingFET shows better immunity against Short Channel Effects by reducing I_{OFF} and providing a higher I_{ON}/I_{OFF} ratio apart from improved threshold voltage roll-off.

4. TCAD based investigation of RingFET architecture has also been performed for evaluating behavior of the device high frequency applications. Parameters such as: cut-off frequency, max. transducer power gain, Stern Stability factor, Unilateral power gain, scattering parameters and parasitic capacitance (i.e. C_{gs} and C_{gd}) are evaluated. Maximum cut-off frequency of 3.7 THz has been achieved with RingFET (having drain outside) architecture at 32nm channel length which is significantly high in comparison to equivalent bulk MOSFET. Due to asymmetric nature of RingFET architecture, lower cut-off frequency is observed in drain inside RingFET (i.e. 3.4 THz) compared to drain outside.

5. To further improve the device electrostatics, another gate has been used at the back side of the device i.e. Double Gate on RingFET (DG-RingFET). Various parameters like drain current (I_{ds}-V_{gs}), trans-conductance (g_m), device efficiency (g_m/I_{ds}), and early voltage (V_{ea}) are explored and compared with single gate RingFET. Linearity behaviour of DG-RingFET has also been assessed in terms of third-order voltage intercept point (VIP_3), third-order current intercept point (IIP_3), third-order inter modulation distortion (IMD_3) for analyzing undesirables harmonics of the device and compared it with the single gate architecture.

6. The impact of gate material engineering on the performance of RingFET architecture i.e. Dual Material Gate RingFET (DMG-RingFET) has also been investigated using ATLAS 3D device simulation for analyzing the performance of the device for digital performance. Different oxide material has been used to further improve the gate controllability instead of using another gate. DMG-RingFET based NMOS-inverter has been simulated and also compared with conventional RingFET based inverter. Since load resistance has been used in NMOS inverter. Thus, different value of load resistances has been used to optimize the bahaviour of the device for better digital performance i.e. higher noise margin and inverter gain. Reliability of the circuit has also been checked under different operating conditions i.e. temperature and bias voltage.

7. Since the detection of gas molecules has also been immensely important now a days. Also, MOSFET based gas sensors and chemical sensors are mostly used because of their low cost.

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The oxygen gas sensor is generally used by drivers to measure the partial pressure of oxygen in their breathing gas. Thus, RingFET based gas sensor can be used to provide good sensitivity compared to planner bulk MOSFET based sensors. Due to the dependency of the partial pressure of the gas on its molar concentration, any change in latter leads to change in work function which results in the variation of device electrical parameters (like I_{off}, and threshold voltage etc.).

8. An open platform modeling-based device simulation module has been developed which can be used by students (under Graduate, Post Graduate and PhD students of Engineering or Applied Science streams) to have a hands-on experience on VLSI. This work focuses on development of GUI based platform. In addition to this the developed platform has web-based interface which gives the user more friendly and versatile environment. The platform has been designed using web2.0 technologies. The frontend is powered by HTML5/CSS3 and JavaScript, while the backend – the core processing and analytics unit – is implemented in PYTHON. Since it is open source license, thus students can easily access this tool in comparison to the existing commercial license tools.

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Appendix F

CONTRIBUTION TO THE SOCIETY

1. Since the detection of gas molecules has also been immensely important now a days. Also, MOSFET based gas sensors and chemical sensors are mostly used because of their low cost. The oxygen gas sensor is generally used by drivers to measure the partial pressure of oxygen in their breathing gas. Thus, RingFET based gas sensor can be used to provide good sensitivity compared to planner bulk MOSFET based sensors. Due to the dependency of the partial pressure of the gas on its molar concentration, any change in latter leads to change in work function which results in the variation of device electrical parameters (like I_{off}, and threshold voltage etc.).

2. RingFET architecture is also used for high frequency application because of high cut-off frequency (in the range of THz) and maximum frequency of oscillation.

3. An open platform modeling-based device simulation module has been developed which can be used by students (under Graduate, Post Graduate and PhD students of Engineering or Applied Science streams) to have a hands-on experience on VLSI. This work focuses on development of GUI based platform. In addition to this the developed platform has web-based interface which gives the user more friendly and versatile environment. The platform has been designed using web2.0 technologies. The frontend is powered by HTML5/CSS3 and JavaScript, while the backend – the core processing and analytics unit – is implemented in PYTHON. Since it is open source license, thus students can easily access this tool in comparison to the existing commercial license tools.

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Appendix G

On the basis of work done, following papers has been published in various international journal and international conferences.

International Journals

1. Sachin Kumar, Vandana Kumari, Sanjeev Singh, Manoj Saxena and Mridula Gupta, "Nanoscale-RingFET: An Analytical drain Current Model including SCE's" IEEE Transactions on Electron Devices, Vol.62(12), pp. 3965 - 3972 Nov. 2015. ISSN No. 0018-9383, DOI: 10.1109/TED.2015.2493578, Impact Factor: 2.512.
2. Sachin Kumar, Vandana Kumari, Sanjeev Singh, Manoj Saxena and Mridula Gupta, "Sub-threshold Drain Current model of Double Gate RingFET (DG-RingFET) Architecture: An Analog and Linearity Performance Investigation for RFIC Design" IETE Technical Review, pp. 1-10, Jan 2017. ISSN No. 0974-5971. Impact Factor: 1.330. DOI: http://dx.doi.org/10.1080/02564602.2016.1270174
3. Sachin Kumar, Vandana Kumari, Sanjeev Singh, Manoj Saxena and Mridula Gupta, "Reconnoiter the leavening of skin-deep insulated extension on analog performance of RingFET (SDIE-RingFET)" International Journal of Electronics and Communications (AEÜ), Vol.83, pp. 67-72, Nov. 2018, ISSN No. 1434-8411, DOI: https://doi.org/10.1016/j.aeue.2017.07.038, Impact Factor: 1.147.

International/National Conferences

4. Sachin Kumar, Vandana Kumari, Manoj Saxena, Mridula Gupta, "Hot Carrier Reliability and linearity Performance Investigation of Nanoscale RinFET for RFIC Design", International Conference on Microwave, Antenna, Propagation and Remote sensing (ICMARS 2013), 11th – 14th December pp. 40-44, Jodhpur, India.
5. Sachin Kumar, Vandana Kumari, Manoj Saxena and Mridula Gupta, "Investigation of III-V Compound Semiconductor Materials on Analog performance of Nanoscale RingFET" Annual IEEE India Conference-INDICON-2015, 17th- 20th Dec. 2015, Delhi, Electronic ISSN: 2325-9418
6. Sachin Kumar, V. Kumari, M. Saxena, and M. Gupta, "TCAD Assessment of Dual Material Gate Nanoscale RingFET (DMG-RingFET) for Analog and Digital Applications" International Conference on Devices Circuit and System-2014, pp. 1-5, Coimbatore, Tamilnadu, India, 2014, **DOI:** 10.1109/ICDCSyst.2014.6926181, ISBN- 978-1-4799-1356-5.
7. Sachin Kumar, Vandana Kumari, Sanjeev Singh, Manoj Saxena and Mridula Gupta, "Impact of High-K Gate Dielectric on Double Gate RingFET (HK-DGRingFET) Architecture", National Conference on Recent Developments in Electronics (NCRDE-2017), pp.177-180, February 17-18, 2017, Delhi, India.
8. Vandana Kumari, Sanjeev Singh, Manoj Saxena and Mridula Gupta "RingFET Architecture for High Frequency Applications: TCAD based Assessment" Communicated in EDKcon-2018.

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