SCHEME OF COURSES – M.TECH. (EMBEDDED SYSTEMS AND VLSI)

UNIVERSITY OF DELHI

NETAJI SUBHAS INSTITUTE OF TECHNOLOGY

Choice Based Credit system

Scheme of Courses

for

Master of Technology

in

Embedded System and VLSI

Electronics and Communication Engineering

SCHEME OF COURSES – M.TECH. (EMBEDDED SYSTEMS AND VLSI)

TABLE OF CONTENTS

S. No.	Contents	Page Number
1.	PREAMBLE	3-12
2.	SEMESTER-WISE COURSE ALLOCATION (Full-Time)	13-15
3.	SEMESTER-WISE COURSE ALLOCATION (Part-Time)	16-18
4.	LIST OF DISCIPLINE CENTRIC ELECTIVES	19-20
5.	LIST OF OPEN ELECTIVES	21
6.	SYLLABUS OF CORE COURSES	22-25
7.	SYLLABUS OF DISCIPLINE CENTRIC ELECTIVE COURSES	26-46
8.	SYLLABUS OF OPEN ELECTIVE COURSES	47-60

PREAMBLE

SCHEME OF COURSES – M.TECH. (EMBEDDED SYSTEMS AND VLSI)

I. INTRODUCTION

Higher education is very important for the growth and development of any country. It is a living organ and requires continuous changes to ensure the quality of education. National Knowledge Commission and University Grants Commission have recommended many academic reforms to address the challenges of today's networked globalized world. People are coming together with the help of new technologies which is resulting towards new aspirations, expectations, collaborations and associations. The concept of "work in isolation" may not be relevant and significant anymore. The UGC guidelines on adoption of Choice Based Credit System may be an important step to revamp the processes, systems and methodologies of Higher Educational Institutions (HEIs). The teacher centric mode be changed to learner centric mode. Class room teaching and learning be made effective; relevant and interesting. Concepts and theories be explained with examples, experimentation and related applications.

A culture of discussions, arguments, interpretations, counter-interpretations, re-interpretations, opposing interpretations must be established. Research should not only be confined to redefinition, extension and incremental change. Innovation & creativity should become an epicenter for all research initiatives. The most important capital is the human capital and thus the ultimate objective is to develop good human beings with utmost integrity & professionalism for this new world.

The Choice Based Credit System supports the grading system which is considered to be better than conventional marks system. It is followed in many reputed institutions in India and abroad. The uniform grading system facilitates student mobility across the institutions within and across the countries and also enable potential employers to assess the performance of the students. The Choice Based Credit System makes the curriculum interdisciplinary and bridge the gap between professional and liberal education.

II. CHOICE BASED CREDIT SYSTEM

The Indian Higher Education Institutions have been moving from the conventional annual system to semester system. Currently many of the institutions have already introduced the choice based credit system. The semester system accelerates the teaching-learning process and enables vertical and horizontal mobility in learning. The credit based semester system provides flexibility in designing curriculum and assigning credits based on the course content and hours of teaching. The choice based credit system provides a 'cafeteria' type approach in which the students can take

courses of their choice, learn at their own pace, undergo additional courses and acquire more than the required credits, and adopt an interdisciplinary approach to learning. It is desirable that the HEIs move to CBCS and implement the grading system.

A. Types of Courses

Courses are the subjects that comprise the M. Tech. programme.

1. A course may be designed to comprise lectures, tutorials, laboratory work, field work, outreach activities, project work, vocational training, viva, seminars, term papers, assignments, presentations, self-study etc. or a combination of some of these components.

2. The learning objectives and learning outcomes of each course will be defined before the start of a semester.

3. Courses are of two kinds: Core and Elective.

    i. **Core Course (CC)**: This is a course which is to be compulsorily studied by a student as a core requirement to complete the requirement of M. Tech.

    ii. **Elective Course**: An elective course is a course which can be chosen from a pool of subjects. It is intended to support the discipline of study by providing an expanded scope, enabling exposure to another discipline/domain and nurturing student's proficiency/skill. An elective may be of following types:

        a) **Discipline Centric Elective (ED)**: It is an elective course that adds proficiency to the students in the discipline.

        b) **Open Elective (EO):** It is an elective course taken from other engineering disciplines that broadens the perspective of an Engineering student.

4. Each course contributes certain credits to the programme. A course can be offered either as a full course (4 credits) or as a half course (2 credits). A full course is conducted with 3 hours of lectures and either 1 hour of tutorial or 2 hours of practical work per week. A half course is conducted with 2 hours of lectures.

5. A student of Postgraduate programme has to accumulate about 40% credits from the Core Courses and the remaining credits from the Elective Courses to become eligible for the award of degree/ diploma/ certificate programmes.

SCHEME OF COURSES – M.TECH. (EMBEDDED SYSTEMS AND VLSI)

6. A course (full/half) may also be designed without lectures or tutorials. However, such courses may comprise Field work, Outreach activities, Project work, Vocational Training, Seminars, Self-study etc. or a combination of some of these.

7. A Project work/ Dissertation is considered as a special course involving application of the knowledge gained during the course of study in exploring, analyzing and solving complex problems in real life applications. A candidate completes such a course on his own with an advisory support by a teacher/faculty member.

B. Examination and Assessment

The following system will be implemented in awarding grades and CGPA under the CBCS system.

1. **Letter Grades and Grade Points:** A 10-pointgradingsystem shall be used with the l etter grades as given in Table 1 below:

Table1: Grades and Grade Points

Letter Grade	Grade point
O (Outstanding)	10
A+ (Excellent)	9
A (Very Good)	8
B+ (Good)	7
B (Above average)	6
C (Average)	5
P (Pass)	4
F (Fail)	0
Ab (absent)	0

2. **Fail grade:** A student obtaining Grade F shall be considered failed and will be required to reappear in the examination. If the student does not want to reappear in an elective subject (that is ED, EO *but not CC courses*) then he/she can re-register afresh for a new elective subject.

3. **Non-credit course:** For non credit courses, 'Satisfactory' or "Unsatisfactory' shall be indicated instead of the letter grade and this will not be counted for the computation of SGPA/CGPA. However, a student must get satisfactory to get the degree.

4. **Fairness in Assessment:** The CBCS promotes continuous evaluation system where end semester examinations weightage should not be more than 60%. The Departments should

SCHEME OF COURSES – M.TECH. (EMBEDDED SYSTEMS AND VLSI)

design their own methods for continuous evaluation. They have the flexibility and freedom in designing the examination and evaluation methods that best fits the curriculum, syllabi & teaching, learning methods. In this regard, the checks and balances be implemented which would enable Departments effectively and fairly carry out the process of assessment and examination.

5. **Computation of SGPA and CGPA:** The following procedure be used to compute the Semester Grade Point Average (SGPA) and Cumulative Grade Point Average (CGPA):

   i. The SGPA is the ratio of sum of the product of the number of credits and the grade points scored in all the courses of a semester, to the sum of the number of credits of all the courses taken by a student, that is:

$$\mathrm{SGPA}(S_i) = \frac{\sum C_j \times G_j}{\sum C_j}$$

   where S_i is the *i*th Semester C_j is the number of credits of the jth course and G_j is the grade point scored by the student in the jth course.

   ii. The CGPA is also calculated in the same manner taking into account all the courses taken by a student over all the semesters of a programme, that is:

$$\mathrm{CGPA} = \frac{\sum C_i \times \mathrm{SGPA}(S_i)}{\sum C_i}$$

   where SPGA(S_i) is the SGPA of the ith semester and C_i is the total number of credits in that semester.

   iii. The SGPA and CGPA shall be rounded off to 2 decimal points and reported in the transcripts.

   iv. CGPA shall be converted in to percentage of marks, if required, by multiplying CGPA with 10.

III. PROGRAMME STRUCTURE

1. The M.Tech. Embedded System and VLSI consists of consists of 4 semesters, normally completed in 2 years for Full-Time and 6 semesters, normally completed in 3 years for Part-Time. The total span period cannot exceed 4 years for Full-Time and 5 years for Part-Time.

SCHEME OF COURSES – M.TECH. (EMBEDDED SYSTEMS AND VLSI)

2. The courses offered in each semester are given in the **Semester-wise Course Allocation.**

3. The discipline centric subjects under CC and ED categories are listed for each discipline separately.

4. A course may have pre-requisite courses that are given in the **Semester-wise Course Allocation**. A student can opt for an elective only if he/she has fulfilled its pre-requisites.

5. A student has to register for all electives before the start of a semester.

IV. COURSE CODIFICATION

The codes for various Postgraduate Programme are as follows:

i. Department of Electronics and Communication Engineering:
   1. Signal Processing-ECSP
   2. Embedded System and VLSI-ECES

ii. Department of Computer Engineering:
   1. Information System-COIS

iii. Department of Instrumentation and Control Engineering:
   1. Process Control-ICPC
   2. Industrial Electronics-ICIE
   3. Mechatronics-ICMT

iv. Department of Biotechnology:
   1. Biochemical Engineering - BTBC
   2. Bioinformatics- BTBF

v. Manufacturing processes and Automation Engineering:
   1. CAD CAM- MACD
   2. Manufacturing process and Automation Engineering.- MAMP
   3. Production Engineering- MAPE
   4. Engineering Management- MAEM
   5. Nanotechnology- MANT

SCHEME OF COURSES – M.TECH. (EMBEDDED SYSTEMS AND VLSI)

The first two letters of the code represent the department, and the remaining two letters represent the course. The codes for Departmental core subjects and Domain-specific Electives are specific to each Discipline.

For I[st] semester, the codes are:

ESC01	CC
ESC02	CC
ESD**	Elective
ESD**	Elective
ESD**	Elective
EO***	Open Elective

For II[nd] semester, the codes are:

ESC03	CC
ESC04	CC
ESD**	Elective
ESD**	Elective
ESD**	Elective
EO***	Open Elective

For III[rd] semester, the codes are:

ESD**	Elective
ESD**	Elective
ESD**	Self-Learning Course
ESC05	Seminar
ESC06	Major Project

SCHEME OF COURSES – M.TECH. (EMBEDDED SYSTEMS AND VLSI)

For IVth semester, the codes are:

ESC07	Dissertation

V. EVALUATION SCHEME

The courses are evaluated on the basis of continuous assessments, mid-semester exams and end-semester exams. The weightage of each of these modes of evaluation for the different types of courses are given is as follows.

Type of Course	**Continuous Assessment (CA), Theory**	**Mid-Semester Exam (MS) Theory**	**End-Semester Exam (ES) Theory**	**Continuous Assessment (CA), Lab**	**End-Semester Exam (ES) Lab**
CC/ED/EO Theory with/ without Tutorial	25	25	50	Nil	Nil
CC/ED/EO Theory with Practical	15	15	40	15	15
Major Project and Dissertation	Nil	Nil	Nil	40	60

VI. DECLARATION OF RESULTS

1. The M.Tech (ES) programme consists of 82 credits. A student will be awarded the degree if he/she has earned all 82 credits.
2. CGPA will be calculated on the basis of the best 78 credits earned by the student.
3. The candidate seeking re-evaluation of a course shall apply for the same on a prescribed proforma along with the evaluation fee prescribed by the university from time to time only for the End Semester Examination within seven days from the date of declaration of result.
4. The Institution/University may cancel the registration of all the courses in a given semester if
   i. The student has not cleared the dues to the institution/hostel.

SCHEME OF COURSES – M.TECH. (EMBEDDED SYSTEMS AND VLSI)

ii. A punishment is awarded leading to cancellation of the student's registration.

VII. EVALUATION AND REVIEW COMMITTEE

The Committee of Courses and Studies in each department shall appoint one or more Evaluation-cum-Review Committees (ERC), each committee dealing with one course or a group of courses. This ERC consists of all faculty members who are likely to teach such courses in the group. Normally Head of the department shall be ERC Chairman.

The ERC has the following functions-

(i) To recommend appointment of paper setters/examiners of various examinations at the start of each semester.

(ii) To prepare quizzes, assignments, test papers etc. for Continuous Assessment (CA), Mid-Semester examination (MS) and End Semester (ES) examination and to evaluate them. Normally, each concerned faculty member, who is also a member of ERC, will do this job for his/her class. However, in exceptional circumstances any part of the work may be entrusted to some other member of the ERC.

(iii) To consider the individual representation of students about evaluation and take remedial action if needed. After scrutinizing, ERC may alter the grades awarded upward/downward. The decision of the ERC shall be final.

(iv) To moderate assignments, quizzes etc. for courses given by each of the concerned faculty members for his/her class with a view to maintain uniformity of standards.

(v) To review and moderate the MS and ES results of each course with a view to maintain uniformity of standards.

(vi) To lay guidelines for teaching a course.

VIII. ATTENDANCE, PROMOTION AND DETENTION RULES

1. A student should normally attend all the classes. However, a student will be allowed to appear in the examination if he/ she has put in a minimum of 75% attendance separately in each course for which he / she has registered. A relaxation up to a maximum of 25% may be given on the production of satisfactory evidence that (a) the student was busy in authorized activities, (b) the student was ill.
2. A student should submit the evidence to the fact 1(a) and / or 1(b) above within seven working days of resuming the studies. Certificates submitted later will not be considered.
3. No relaxation in attendance beyond 25% is permitted in any case.

SCHEME OF COURSES – M.TECH. (EMBEDDED SYSTEMS AND VLSI)

4. A student may re-register for a course if he/ she want to avoid a decrement in the grades.
5. There shall be no supplementary examinations. A student who has failed in a course will have to re-register for the course in a subsequent year.
6. If the student does not want to reappear in an elective course (that is, ED, EO, but not CC courses) then he/she can re-register afresh for a new elective course.

IX. CURRICULUM MODIFICATION

The curriculum will be updated regularly within a period of 5 to 10 years since last revision, to keep pace with the advancements in the field of Biochemical Engineering.

X. CENTRAL ADVISORY COMMITTEE

There shall be a Central Advisory Committee consisting of the following—

a) Dean, Faculty of Technology, Chairman
b) Dean PGS
c) Head of Institution
d) Heads of Departments running M. Tech Courses

XI. PROGRAM EDUCATIONAL OBJECTIVE:

The major objectives of the M. Tech programme in Embedded System and VLSI are to equip the students with adequate knowledge and skills in Embedded System and VLSI to prepare them for the following career options:

1. Provide graduates with a strong foundation in Embedded System and VLSI fundamentals to enable them to devise and deliver efficient solutions to challenging problems in Electronics, and allied disciplines.

2. Practice the ethics of their profession consistent with a sense of social responsibility and develop their engineering design, problem –solving skills and aptitude for innovations and research as they work individually and in multi disciplinary teams.

SCHEME OF COURSES – M.TECH. (EMBEDDED SYSTEMS AND VLSI)

3. Be receptive to new technologies and attain professional competence through lifelong learning such as doctoral degree, professional registration, publications and other professional activities.

XII. PROGRAM OUTCOMES

1. Capability of applying knowledge of Embedded System and VLSI to solve Electronics Engineering problems.
2. Ability to create suitable models of complex systems and analyze them.
3. Capability to design/conduct experiments and draw inference and conclusions there from.
4. Ability to provide/devise solutions for engineering problems related to the needs of the Industries and Society.
5. Ability to apply knowledge of Embedded System and VLSI to develop useful products/prototypes/hardware/software.
6. Capability to understand professional and ethical responsibilities.
7. Capability to communicate effectively, orally as well as in writing.
8. Ability to work independently as well as part of teams.

SCHEME OF COURSES – M.TECH. (EMBEDDED SYSTEMS AND VLSI)

SEMESTER-WISE COURSE ALLOCATION (Full-Time)

M.TECH. EMBEDDED SYSTEM AND VLSI (Full Time) SEMESTER I

CODE	TYPE	COURSE OF STUDY	L	T	P	C	EVALUATION SCHEME Percentage (Weightage)					
							Theory			Practical		Total
							CA	MS	ES	CA	ES	
ESC01	CC	CMOS Analog Circuit Design	3	0	2	4	15	15	40	15	15	100
ESC02	CC	Microcontrollers for Embedded System Design	3	0	2	4	15	15	40	15	15	100
ESD**	ED	Elective #	-	-	-	4	-	-	-	-	-	100
ESD**	ED	Elective #	-	-	-	4	-	-	-	-	-	100
ESD**	ED	Elective #	-	-	-	4	-	-	-	-	-	100
EO***	EO	Open Elective #	3	1	0	4	25	25	50	-	-	100
		TOTAL	-	-	-	24						
			$									

The LTP allocation, Evaluation scheme and pre- requisites for Electives are given in Table 2-3. The course code will depend upon student's choice of elective(s).
$ The actual weekly load will depend upon the elective(s) chosen by the student.

SCHEME OF COURSES – M.TECH. (EMBEDDED SYSTEMS AND VLSI)

M.TECH. EMBEDDED SYSTEM AND VLSI (Full Time) SEMESTER II

CODE	TYPE	COURSE OF STUDY	L	T	P	C	EVALUATION SCHEME Percentage (Weightage)					
							Theory			Practical		Total
							CA	MS	ES	CA	ES	
ESC03	CC	Integrated Circuits for Analog Signal Processing	3	0	2	4	15	15	40	15	15	100
ESC04	CC	Processor Design	3	0	2	4	15	15	40	15	15	100
ESD**	ED	Elective #	-	-	-	4	-	-	-	-	-	100
ESD**	ED	Elective #	-	-	-	4	-	-	-	-	-	100
ESD**	ED	Elective #	-	-	-	4	-	-	-	-	-	100
EO***	EO	Open Elective #	3	1	0	4	25	25	50	-	-	100
		TOTAL	-	-	-	24						
			$									

The LTP allocation, Evaluation scheme and pre- requisites for Electives are given in Table 2-3. The course code will depend upon student's choice of elective(s).
$ The actual weekly load will depend upon the elective(s) chosen by the student.

SCHEME OF COURSES – M.TECH. (EMBEDDED SYSTEMS AND VLSI)

M.TECH. EMBEDDED SYSTEM AND VLSI (Full Time) SEMESTER III

CODE	TYPE	COURSE OF STUDY	L	T	P	C	EVALUATION SCHEME Percentage (Weightage)					
							Theory			Practical		Total
							CA	MS	ES	CA	ES	
ESC05	CC	Seminar	-	-	-	2	100	-	-	-	-	100
ESC06	CC	Major Project	-	-	-	6				40	60	100
ESD**	ED	Elective #	-	-	-	4	-	-	-	-	-	100
ESD**	ED	Elective#	-	-	-	4	-	-	-	-	-	100
ESD**	ED	Elective#	-	-	-	4	-	-	-	-	-	100
		TOTAL	-	-	-	20						
			$									

The LTP allocation, Evaluation scheme and pre- requisites for Electives are given in Table 2-3. The course code will depend upon student's choice of elective(s).
$ The actual weekly load will depend upon the elective(s) chosen by the student.

M.TECH. EMBEDDED SYSTEM AND VLSI (Full Time) SEMESTER IV

CODE	TYPE	COURSE OF STUDY	L	T	P	C	EVALUATION SCHEME Percentage (Weightage)					
							Theory			Practical		Total
							CA	MS	ES	CA	ES	
ESC07	CC	Dissertation	-	-	-	14	-	-	-	40	60	100
		TOTAL	-	-	-	14						

SCHEME OF COURSES – M.TECH. (EMBEDDED SYSTEMS AND VLSI)

SEMESTER-WISE COURSE ALLOCATION (Part-Time)

M.TECH. EMBEDDED SYSTEM AND VLSI (Part Time) SEMESTER I

CODE	TYPE	COURSE OF STUDY	L	T	P	C	EVALUATION SCHEME Percentage (Weightage)					
							Theory			Practical		Total
							CA	MS	ES	CA	ES	
ESC01	CC	CMOS Analog Circuit Design	3	0	2	4	15	15	40	15	15	100
ESC02	CC	Microcontrollers for Embedded System Design	3	0	2	4	15	15	40	15	15	100
EO***	EO	Open Elective #	3	1	0	4	25	25	50	-	-	100
		TOTAL	9	1	4	12						

M.TECH. EMBEDDED SYSTEM AND VLSI (Part Time) SEMESTER II

CODE	TYPE	COURSE OF STUDY	L	T	P	C	EVALUATION SCHEME Percentage (Weightage)					
							Theory			Practical		Total
							CA	MS	ES	CA	ES	
ESC03	CC	Integrated Circuits for Analog Signal Processing	3	0	2	4	15	15	40	15	15	100
ESC04	CC	Processor Design	3	0	2	4	15	15	40	15	15	100
EO***	EO	Open Elective #	3	1	0	4	25	25	50	-	-	100
		TOTAL	9	1	4	12						

SCHEME OF COURSES – M.TECH. (EMBEDDED SYSTEMS AND VLSI)

M.TECH. EMBEDDED SYSTEM AND VLSI (Part Time) SEMESTER III

CODE	TYPE	COURSE OF STUDY	L	T	P	C	EVALUATION SCHEME Percentage (Weightage)					
							Theory			Practical		Total
							CA	MS	ES	CA	ES	
ESD**	ED	Elective #	-	-	-	4	-	-	-	-	-	100
ESD**	ED	Elective #	-	-	-	4	-	-	-	-	-	100
ESD**	ED	Elective #	-	-	-	4	-	-	-	-	-	100
		TOTAL	-	-	-	12						
			$									

The LTP allocation, Evaluation scheme and pre- requisites for Electives are given in Table 2-3. The course code will depend upon student's choice of elective(s).
$ The actual weekly load will depend upon the elective(s) chosen by the student.

M.TECH. EMBEDDED SYSTEM AND VLSI (Part Time) SEMESTER IV

CODE	TYPE	COURSE OF STUDY	L	T	P	C	EVALUATION SCHEME Percentage (Weightage)					
							Theory			Practical		Total
							CA	MS	ES	CA	ES	
ESD**	ED	Elective #	-	-	-	4	-	-	-	-	-	100
ESD**	ED	Elective #	-	-	-	4	-	-	-	-	-	100
ESD**	ED	Elective #	-	-	-	4	-	-	-	-	-	100
		TOTAL	-	-	-	12						
			$									

The LTP allocation, Evaluation scheme and pre- requisites for Electives are given in Table 2-3
. The course code will depend upon student's choice of elective(s).
$ The actual weekly load will depend upon the elective(s) chosen by the student.

SCHEME OF COURSES – M.TECH. (EMBEDDED SYSTEMS AND VLSI)

M.TECH. EMBEDDED SYSTEM AND VLSI (Part Time) SEMESTER V

CODE	TYPE	COURSE OF STUDY	L	T	P	C	EVALUATION SCHEME Percentage (Weightage)					
							Theory			Practical		Total
							CA	MS	ES	CA	ES	
ESC06	CC	Major Project	-	-	-	6				40	60	100
ESD**	ED	Elective #	-	-	-	4	-	-	-	-	-	100
ESD**	ED	Elective #	-	-	-	4	-	-	-	-	-	100
		TOTAL	-	-	-	14						
			$									

The LTP allocation, Evaluation scheme and pre- requisites for Electives are given in Table 2-3. The course code will depend upon student's choice of elective(s).
$ The actual weekly load will depend upon the elective(s) chosen by the student.

M.TECH. EMBEDDED SYSTEM AND VLSI (Part Time) SEMESTER VI

CODE	TYPE	COURSE OF STUDY	L	T	P	C	EVALUATION SCHEME Percentage (Weightage)					
							Theory			Practical		Total
							CA	MS	ES	CA	ES	
ESC05	CC	Seminar	-	-	-	2	100	-	-	-	-	100
ESC07	CC	Dissertation	-	-	-	14	-	-	-	40	60	100
ESD**	ED	Elective #	-	-	-	4	-	-	-	-	-	100
		TOTAL	-	-	-	20						
			$									

$ The actual weekly load will depend upon the elective(s) chosen by the student.

SCHEME OF COURSES – M.TECH. (EMBEDDED SYSTEMS AND VLSI)

Table 2: LIST OF DISCIPLINE CENTRIC ELECTIVES

CODE	COUSRE OF STUDY	PREREQUISITE	L	T	P	C
ESD01	Embedded System Design	____	3	1/0	0/2	4
ESD02	Embedded Real Time Operating Systems	____	3	1/0	0/2	4
ESD03	Switched-Capacitor and Switched-Current Circuits	____	3	1/0	0/2	4
ESD04	Semiconductor Devices	____	3	1/0	0/2	4
ESD05	Device Modelling and Circuit Simulation	____	3	1/0	0/2	4
ESD06	Digital Integrated Circuits	____	3	1/0	0/2	4
ESD07	Digital System Design using HDLs	____	3	1/0	0/2	4
ESD08	Optimization Techniques	____	3	1/0	0/2	4
ESD09	Embedded Networking	ESD01	3	1/0	0/2	4
ESD10	Sensors and Actuators	____	3	1/0	0/2	4
ESD11	Hardware Software Co-design	ESD01	3	1/0	0/2	4
ESD12	Modern Analog Filter Design	ESC01	3	1/0	0/2	4
ESD13	Deep Sub Micron CMOS ICs	ESD04	3	1/0	0/2	4
ESD14	ASIC Design	ESD07	3	1/0	0/2	4
ESD15	Design of Semiconductor Memories	ESD06	3	1/0	0/2	4
ESD16	Algorithms for VLSI Design Automation	ESD07	3	1/0	0/2	4

SCHEME OF COURSES – M.TECH. (EMBEDDED SYSTEMS AND VLSI)

ESD17	Low Power VLSI Design	ESD06, ESC01	3	1/0	0/2	4
ESD18	Neural networks in embedded applications	ESC01	3	1/0	0/2	4
ESD19	Internet of Things	ESD09, ESD10	3	1/0	0/2	4
ESD20	Current Mode Techniques for Signal Processing	ESC01	3	1/0	0/2	4
ESD21	System on Chip Design	ESC01, ESD06	3	1/0	0/2	4
ESD22	Scripting Languages for Design Automation	___	3	1/0	0/2	4
ESD23	Optimization of CMOS Integrated Circuits	ESC01, ESD06	3	1/0	0/2	4
ESD24	Soft Computing Techniques	___	3	1/0	0/2	4
ESD25	Mixed Signal IC Design	ESC01, ESD06	3	1/0	0/2	4
ESD26	Design for testability	ESD06	3	1/0	0/2	4

SCHEME OF COURSES – M.TECH. (EMBEDDED SYSTEMS AND VLSI)

Table 3: LIST OF OPEN ELECTIVES

LTP Allocation			Evaluation Scheme				
			Theory			Practical	
L	T	P	CA	MS	ES	CA	MS
3	1	0	25	25	50	-	-
Code	**Name of Elective**		**Pre-Requisites**				
EO001	Technical Communication		None				
EO002	Disaster Management		None				
EO003	Basics of Finance Management		None				
EO004	Basics of Human Resources Management		None				
EO005	Project Management		None				
EO006	Basics of Corporate Law		None				
EO007	Biological computing		None				
EO008	Sociology		None				
EO009	Entrepreneurship		None				
EO010	Social work		None				
EO011	IP and Patenting		None				
EO012	Supply Chain Management-Planning and logistics		None				
EO013	Organization Development		None				
EO014	Industrial Organisation and Managerial Economics		None				
EO015	Global Strategy and Technology		None				
EO016	Engineering System Analysis and Design		None				
EO017	Biology for Engineers		None				
EO018	Energy, Environment and Society		None				
EO019	Public Policy and Governance		None				

SCHEME OF COURSES – M.TECH. (EMBEDDED SYSTEMS AND VLSI)

SYLLABUS OF CORE COURSES

Course Code	Course Name	Course Structure	Pre-Requisite
ESC01	CMOS Analog Circuit Design	L-T-P 3-0-2	___
COURSE OUTCOME (CO): CO-1: To understand the operation of CMOS devices and its use as an amplifier. CO-2: To become familiar with the small- and large-signal models of CMOS transistors. CO-3: To analyze the building blocks of analog circuits such as current mirrors and differential amplifiers. CO-4: To understand the concepts of gain, power, bandwidth, noise and study the effects of feedback.			
COURSE CONTENT: Biasing in MOS amplifier circuits, small signal equivalent circuit model, Single stage MOS amplifiers, characterizing amplifiers, MOS internal capacitance and high frequency model, frequency response. IC biasing-current sources, current mirrors and current-steering circuits, cascode and wilson current mirror, Common Source, common gate and common drain IC amplifiers, low frequency and high frequency response, noise performance, Multiple-Transistor IC amplifiers, Cascode configuration, folded cascode and self cascode structure, Voltage follower, flipped voltage follower. MOS differential pair, small signal operation, differential gain ,common mode gain, common mode rejection ration, non ideal characteristics, active loaded differential amplifier, Frequency response, Noise Spectrum, sources, types, Thermal and Flicker noise, representation in circuits, Noise bandwidth, Noise figure. General feedback structure, negative feedback, four basic topologies, loop gain, stability, effect of feedback on amplifier poles, single pole response, two pole response, Frequency compensation, Compensation Techniques, Pole splitting			
SUGGESTED READING: 1. Sedra and Smith, “Microelectronic circuits,” Oxford University press. 2. Kenneth R. Laker and Willy M.C. Sansen, “Design of Analog Integrated Circuits and systems,” McGraw-Hill. 3. Philip E. Allen & Douglas R. Holberg, “CMOS Analog Circuit Design,” Oxford University Press. 4. Behzad Razavi, “Design of Analog CMOS Integrated Circuit,” Tata-McGraw Hill. 5. Gray R.Paul, Hurst J. Paul, Lewis H. Stephen and Meyer G. Robert, “Analysis and Design of Analog Integrated Circuits,” John Wiley and Sons.			

Course Code	Course Name	Course Structure	Pre-Requisite
ESC02	Microcontrollers for Embedded System Design	L-T-P 3-0-2	____
COURSE OUTCOME (CO):			

SCHEME OF COURSES – M.TECH. (EMBEDDED SYSTEMS AND VLSI)

CO-1: To get familiar with the architecture of ARM processor families. CO-2: To understand the various types of instructions and get a grasp over the instruction set. CO-3: To comprehend the concepts for programming the microcontroller. CO-4: To get acquainted with the cache architecture and related issues.
COURSE CONTENT: ARM Design Philosophy, Registers, Program Status Register, Instruction Pipeline, Interrupts and Vector Table, Architecture Revision, ARM Processor Families. Instruction Set: Data Processing Instructions, Addressing Modes, Branch, Load, Store Instructions,PSR Instructions, Conditional Instructions. Thumb Instruction Set: Register Usage, Other Branch Instructions, Data Processing Instructions, Single-Register and Multi Register Load-Store Instructions, Stack, Software Interrupt Instructions. Simple C Programs using Function Calls, Pointers, Structures, Integer and Floating Point Arithmetic, Assembly Code using Instruction Scheduling, Register Allocation, Conditional Execution and Loops. Cache Architecture, Policies, Flushing and Caches, MMU, Page Tables, Translation, Access Permissions, Context Switch.
SUGGESTED READING: 1. Andrew N. Sloss, Dominic Symes, Chris Wright, "ARM Systems Developer's Guides- Designing & Optimizing System Software ," Elsevier. 2. Jonathan W. Valvano–Brookes / Cole, "Embedded Microcomputer Systems, Real Time Interfacing," Thomas Learning.

Course Code	Course Name	Course Structure	Pre-Requisite
ESC03	Integrated Circuits for Analog Signal Processing	L-T-P 3-0-2	_____
COURSE OUTCOME (CO): CO-1: To introduce analogue signal processing techniques that can be used to perform computation in the analogue front end prior to back end processing and/or communication, CO-2: To inculcate the ability to understand increased signal integrity and to reduce the power consumption of the system as whole. CO-3: To understand the various types of noise and their interference in signal. CO-4: To understand voltage and current mode architectures used in analog signal processing. CO-5: Design circuits capable of performing low power analog computation and processing of signals in CMOS. CO-6: Describe circuit techniques which allow efficient computation and signal processing in CMOS.			
COURSE CONTENT: Signals, Information, Interference and noise, signal classification, dynamic range, S/N ratio, Functions in analog signal processing, linear non linear fuctions, impedance adaptation, amplitude and level matching, terminal matching, buffering filtering, linearization, domain conversions, errors in analog			

SCHEME OF COURSES – M.TECH. (EMBEDDED SYSTEMS AND VLSI)

signal processing

Voltage amplification, practical voltage amplifiers, effects of finite input impedances, building blocks for voltage amplifiers, Current to voltage and voltage to current conversion, current integrators, mirrors, amplifiers, conveyors

CMOS analog integrated circuits, analog building blocks, Op-amp design, practical opamp characteristics and model, DC offset and DC bias currents, Gain, bandwidth and slew rate, Noise, Input stage, output stage, CMOS OTA, ideal model, OTA building block circuits, design of simple OTA

Signal rectifications, AC/DC conversion, CMOS implementation of adder, subtractor, squarer, analog multiplier, analog dividers, differentiator and integrator circuits, Impedance transformation and conversion, Analog multiplexers

SUGGESTED READING:

1. Pallas Areny and John G. Webster, "Analog Signal Processing," John Wiley.
2. Tlelo-Cuautle, Esteban (Ed.), "Integrated Circuits for Analog Signal Processing," Springer.
3. Ismail, Mohammed, Sawan, Mohamad ,"Analog Circuits and Signal Processing," The Springer International Series in Engineering and Computer Science.
4. M. Ismail and T. Fiez, "Analog VLSI signal and Information processing," Mc-Graw hill.

Course Code	Course Name	Course Structure	Pre-Requisite
ESC04	Processor Design	L-T-P 3-0-2	_____

COURSE OUTCOME (CO):

CO-1: To understand the major components of embedded computer including CPU, memory, I/O and storage

CO-2: To provide students with a fundamental knowledge of computer hardware and computer systems, with an emphasis on system design and performance.

CO-3: To make the students aware of various processors, their usage and extensibilities.

CO-4: To understand the difference in architecture of asynchronous processors and various design issues involved with it.

COURSE CONTENT:

Embedded Computer Architecture Fundamentals: Components of an embedded computer, Architecture organization, ways of parallelism, I/O operations and peripherals. Problems, Fallacies, and Pitfalls in Processor Design for a high level computer instruction set architecture to support a specific language or language domain, use of intermediate ISAs to allow a simple machine to emulate its betters, stack machines ,overly aggressive pipelining ,unbalanced processor design, Omitting pipeline interlocks, Non-power-of-2 data-word widths for general-purpose computing

Memory: Organization, Memory segmentation, Multithreading, Symmetric multiprocessing.

Processor Design flow: Capturing requirements, Instruction coding, Exploration of architecture organizations, hardware and software development. Extreme CISC and extreme RISC, Very long instruction word (VLIW),

SCHEME OF COURSES – M.TECH. (EMBEDDED SYSTEMS AND VLSI)

Digital signal processor: Digital signal processor and its design issues, evolving architecture of DSP, next generation DSP.

Customizable processors: Customizable processors and processor customization, A benefit analysis of processor customization, use of microprocessor cores in SOC design, benefits of microprocessor extensibility.

Run time Re-configurable Processors: Run time Re-configurable Processors,Embedded microprocessor trends, instruction set metamorphosis, reconfigurable computing, run-time reconfigurable instruction set processors ,coarse grain reconfigurable processors,

Processor Clock Generation and Distribution: Clock parameters and trends, Clock distribution networks, de-skew circuits, jitter reduction techniques, low power clock distribution

Asynchronous Processor Design: Asynchronous and self timed processor design, need of asynchronous design, development of asynchronous processors, asynchronous design styles, features of asynchronous design.

SUGGESTED READING:

1. Jari Nurmi, “Processor Design-System on Chip Computing for ASICs and FPGA,” Springer Publications.
2. G. Frantz, “The DSP and Its Impact on the Technology,” Springer.
3. S. Leibson, “Customizable Processors and Processor Customization,” Springer.

SCHEME OF COURSES – M.TECH. (EMBEDDED SYSTEMS AND VLSI)

SYLLABUS OF DISCIPLINE CENTRIC ELECTIVE COURSES

Course Code	Course Name	Course Structure	Pre-Requisite
ESD01	Embedded System Design	L - T - P 3 - 1/0 - 0/2	____
COURSE OUTCOME (CO): CO-1: To develop basic understanding of embedded systems in general and their applications. CO-2: To comprehend the architecture and components of embedded systems. CO-3: To understand the onboard and external communication interfaces. CO-4: To understand the concepts of multiprocessing, multitasking and shared memory.			
COURSE CONTENT: Definition of Embedded System, Embedded Systems Vs General Computing Systems, History of Embedded Systems, Classification, Major Application Areas, Purpose of Embedded Systems, Characteristics and Quality Attributes of Embedded Systems. Core of the Embedded System: General Purpose and Domain Specific Processors, ASICs, PLDs, Commercial Off-The-Shelf Components (COTS), Memory: ROM, RAM, Memory according to thetype of Interface, Memory Shadowing, Memory selection for Embedded Systems, Sensors and Actuators, Communication Interface: Onboard and External Communication Interfaces. Reset Circuit, Brown-out Protection Circuit, Oscillator Unit, Real Time Clock, Watchdog Timer, Embedded Firmware Design Approaches and Development Languages. Operating System Basics, Types of Operating Systems, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling. Shared Memory, Message Passing, Remote Procedure Call and Sockets, Task Synchronization: Task Communication/Synchronization Issues, Task Synchronization Techniques, Device Drivers, How to Choose an RTOS.			
SUGGESTED READING: 1. Shibu K.V., “Introduction to Embedded Systems,” McGraw Hill. 2. Raj Kamal, “ Embedded Systems,” Tata McGraw Hill. 3. Frank Vahid, Tony Givargis, “Embedded System Design,” John Wiley. 4. Lyla, “Embedded Systems,” Pearson. 5. David E. Simon, “An Embedded Software Primer,” Pearson Education.			

Course Code	Course Name	Course Structure	Pre-Requisite
ESD02	Embedded Real Time Operating Systems	L - T - P 3 - 1/0 - 0/2	_____
COURSE OUTCOME (CO): CO-1: Describe the differences between the general computing system and the embedded system, also recognize the classification of embedded systems.			

SCHEME OF COURSES – M.TECH. (EMBEDDED SYSTEMS AND VLSI)

CO-2: Become aware of the architecture of the ATOM processor and its programming aspects (assembly Level) CO-3: Become aware of interrupts, hyper threading and software optimization. CO-4: Design real time embedded systems using the concepts of RTOS. CO-5: Analyze various examples of embedded systems based on ATOM processor.
COURSE CONTENT: Introduction to Embedded systems, Embedded system vs general Computing system, Classification of Embedded system, Core of Embedded system, RISC vs CISC controllers, Harvard vs Van Neumen architecture. IA 32: Block diagram description and functions of each unit. Atom processor-Addressing modes, Registers, Memory accesses, memory map, Instruction set, Segmentation. Task switching, Paging, Hyper-threading, Caches and TLB, Execution pipeline, Interrupts, Software optimization, VT. FSB Architecture. Chipset over view. BIOS Configuration and responsibilities. BOOT up sequence. Operating system overview, Operating system concepts. Processes, Tasks and Threads, Scheduling, Memory allocation, Clocks and timers, Inter task synchronization, Device driver models, Bus drivers. Power management, Examples and overview of Real time OS. Case studies of embedded systems using Atom processors.
SUGGESTED READING: 1. Raj Kamal, "Embedded Systems Architecture, Programming, and Design," Tata McGraw Hill. 2. K.V. Shibu, "Introduction To Embedded Systems," Tata McGraw Hill.

Course Code	Course Name	Course Structure	Pre-Requisite
ESD03	Switched-Capacitor and Switched-Current Circuits	L - T - P 3 - 1/0 - 0/2	____
COURSE OUTCOME (CO): CO-1: To understand the operation of first and second order switched capacitor circuits. CO-2: To get acquainted with the non-ideal effects and noise generated in switched capacitor circuits. CO-3: To understand the non filtering application of switched capacitor circuits- gain stages, programmable capacitor arrays. CO-4: To comprehend switched capacitor to switched current conversion method.			
COURSE CONTENT: Resistor Emulation (Series, parallel Series-parallel Bilinear, Stray insensitive realizations) Analysis using charge conservation law, (Z domain models for two phase switched capacitor circuits), (Z domain equivalent) admittance approach. Analysis of first order switched capacitor circuits (amplifiers, integrators, differentiators, etc.) Non ideal effects in Switched capacitor circuits (Non ideal effects in switches, capacitance inaccuracies, nonideal opamp circuit effects,) Noise generated in switched capacitor circuits. Second order switched capacitor filters, cascaded filter design, SC ladder filter design.			

SCHEME OF COURSES – M.TECH. (EMBEDDED SYSTEMS AND VLSI)

Non filtering application of switched capacitor circuits- gain stages, programmable capacitor arrays, DI/A and A/D converters, modulators, rectifiers, oscillators phase shifters, comparators, peak detector etc

Profiteering and post filtering requirements for switched capacitor filters.

Switched current systems-Delay module, current memory cell, delay cell, Delay line, Integrator modules & non inverting integrator inverting damped integrators non inverting damped integrator, Generalized integrator, comparison with switched capacitor Integrator, integrator based biquadratic section

Differentiator modules switched current amplifiers Differentiator based biquadratic section, switched capacitor to switched current conversion method:

Biquad switched current filter sections, Ladder filter,Switched current limitation and non ideal behavior –mismatch errors Non unity current gain memory, output input conductance ratio errors, setting error.

SUGGESTED READING:

1. Raj Senani, D. R. Bhaskar, V. K. Singh, R. K. Sharma, "Sinusoidal Oscillators and Waveform Generators using Modern Electronic Circuit Building Blocks," Springer.
2. Chris Toumazou, John B. Hughes, "Switched-currents: An Analogue Technique for Digital Technology," IEE Circuits and Systems Series 5.
3. Rolf Unbehauen, Andrzej Cichocki, "MOS Switched-Capacitor and Continuous- Time Integrated Circuits and Systems," Springer.

Course Code	Course Name	Course Structure	Pre-Requisite
ESD04	Semiconductor Devices	L - T - P 3 - 1/0 - 0/2	____

COURSE OUTCOME (CO):

CO-1: To understand the basic phenomena in semiconductor devices.

CO-2: To get familiar with modern VLSI devices.

CO-3: To understand the operation of emerging transistor technologies.

CO-4: To develop strong understanding of the underlying physics of modern-day VLSI devices.

COURSE CONTENT:

Elemental and compound semiconductors, narrow & wide energy gap semiconductors, direct & indirect semiconductors, choice of semiconductors for specific applications, review of semiconductor fundamentals, energy band, Carrier transport phenomena, Recombination and generation, surface effects, traps.

PN junction, Schottky junctions, Ohmic contacts, BJT device Design, nonideal effects, frequency limitations, MOSFET Operation, subthreshold conduction, mobility variation, velocity saturation threshold voltage modifications, threshold adjustment by Ion implantation, Lightly doped drain MOS transistor, breakdown voltage, radiations and hot electron effects.

Introduction to modern VLSI Devices, Polysilicon emitter transistors, Heterojunctions, 2D electron gas,

SCHEME OF COURSES – M.TECH. (EMBEDDED SYSTEMS AND VLSI)

band alignment, SOI MOSFETs, PDSOI, FDSOI, Source/drain engineering, Brief introduction to HEMTs, MESFET(Metal semiconductor FET) and MODFET(Modulation doped FET).

New VLSI device structures, from bulk to SOI to multi-gate, double gate MOSFET, FinFET, SiGe technology, strain influence on electron mobility, strain enhanced Si based transistors, strained Si CMOS, SiGe HBTs, SiGe MODFETs, Nanowires

SUGGESTED READING:

1. Donald A. Neamen, "Semiconductor Physics and devices," Tata McGraw Hill.
2. Taur and Ning, "Fundamentals of Modern VLSI Devices," Cambridge Press.
3. Ben G. Streetman & S. Banerjee, "Solid state electronic devices," Prentice Hall of India.

Course Code	Course Name	Course Structure	Pre-Requisite
ESD05	Device Modelling and Circuit Simulation	L - T - P 3 - 1/0 - 0/2	____

COURSE OUTCOME (CO):

CO-1: To develop strong understanding of the underlying physics of MOSFETs.
CO-2: To get familiar with small and large signal modelling and modeling for RF applications of MOSFETs.
CO-3: To develop strong understanding of SPICE models.
CO-4: To gain an insight into circuit simulation techniques like DC, AC and transient analyses.

COURSE CONTENT:

Overview of MOS transistor physics, Two-Terminal MOS structure, Flat -band voltage, Effect of Gate-substrate voltage on surface condition, Inversion, Small signal capacitance, Three-Terminal MOS structure, Body effect, regions of inversion, Pinch-off voltage, Four Terminal MOS Transistor, regions of inversion, charge sheet model, interpolation model, body referenced model

MOS transistor large-signal modeling, quasi-static operation, limitations of quasi-static model, introduction to non-quasi static model, MOS transistor small-signal modeling, low & medium frequency model, high frequency model, considerations in MOS modeling for RF applications, gate resistance, transition frequency, maximum frequency of oscillation, Noise model

MOSFET modeling for circuit simulation, Types of models, system for data acquisition and parameter extraction, properties of good models, Introduction to SPICE modeling, modeling of resistor, capacitor, inductor, diode, BJT, JFET, MOSFET, model parameters, Brief overview of BSIM and EKV model , Device and process simulator

Circuit simulation techniques, DC analysis, AC analysis, transient analysis, SPICE Modeling of Process Variation, Process corners, Monte Carlo simulation, and sensitivity/worst case analysis, Simulation of digital and analog circuits, transfer function, frequency response, Noise analysis, distortion and spectral analysis

SUGGESTED READING:

1. Y. Tsividis, "Operation and modeling of MOS transistors," McGRAW-Hill.
2. Paul W. Tuinenga, "SPICE: A Guide to Circuit Simulation and Analysis Using PSpice," Pearson.
3. Paolo Antognetti and Giuseppe Massobrio, "Semiconductor Device Modeling with SPICE,"McGraw-

SCHEME OF COURSES – M.TECH. (EMBEDDED SYSTEMS AND VLSI)

Hill.

Course Code	Course Name	Course Structure	Pre-Requisite
ESD06	Digital Integrated Circuits	L - T - P 3 - 1/0 - 0/2	_____
COURSE OUTCOME (CO): CO-1: To develop strong understanding of the underlying physics of MOSFETs. CO-2: To get familiar with small and large signal modelling and modeling for RF applications of MOSFETs. CO-3: To develop strong understanding of SPICE models. CO-4: To gain an insight into circuit simulation techniques like DC, AC and transient analyses.			
COURSE CONTENT: MOS transistor as switch, CMOS inverter, static behavior, switching threshold, noise margins, dynamic behavior, propagation delay, CMOS inverter power consumption, static and dynamic power, energy-delay analysis, technology scaling and its impact on inverter metrics Static CMOS logic, Pseudo-NMOS logic, pass transistors, complementary pass logic, CMOS transmission-gate logic, differential CMOS logic, transistor sizing, Logical effort, dynamic CMOS logic, dynamic CMOS circuit techniques, high performance dynamic CMOS circuits, charge sharing, design and implementation of Combinational CMOS circuits Sequential MOS logic circuits, timing metrics for sequential circuits, bistability principle, static latches and flip flops, CMOS edge triggered FFs, registers, ratioed and ratioless logic, dynamic latches and registers, pipelining, optimization of sequential circuits, Nonbistable sequential circuits, Schmitt trigger Timing issues in digital circuits, timing classification, choosing a clocking strategy, sources of skew and jitter, clock distribution techniques, self timed circuit, synchronizers and arbiters, distributed clocking, Introduction to BiCMOS and GaAs logic family			
SUGGESTED READING: 1. Jan M. Rabaey, Ananthachandrakasan, Borivojenikolic, "Digital Integrated Circuits-A design perspective," Pearson. 2. Sung Mo Kang, Yusuf Lablebici, "CMOS Digital Integrated Circuits Analysis & Design," Tata Mc-Graw Hill. 3. Ken Martin, "Digital Integrated Circuit Design," Oxford University Press.			

Course Code	Course Name	Course Structure	Pre-Requisite
ESD07	Digital System Design using HDLs	L - T - P 3 - 1/0 - 0/2	_____
COURSE OUTCOME (CO): CO-1: Foster ability to identify and code the module using different modeling styles in VHDL and verilog.			

SCHEME OF COURSES – M.TECH. (EMBEDDED SYSTEMS AND VLSI)

CO-2: Foster ability to write test benches in VHDL/Verilog. CO-3: Acquired knowledge about FSMs and ASMs and how to code controllers using FSMs and ASMs CO-4: Ability to develop synthesizable code in VHDL/Verilog.
COURSE CONTENT: Introduction to VHDL, behavioral, data flow, structural models, simulation cycles, process, concurrent & sequential statements, loops, delay models, library, packages, functions, procedures, test bench, design of digital circuits using VHDL Introduction to Verilog HDL, hierarchical modeling concepts, Lexical conventions, data types, system tasks and compiler directives, modulus and ports, variable, arrays, tables, operators, expressions, signal assignments, nets, registers, concurrent & sequential constructs, tasks & functions Gate-level, Dataflow and behavioral modeling using Verilog HDL, advanced Verilog topics, timing and delays, delay models, path delay modeling, timing checks, switch level modeling, user defined primitives, programming language interface Logic Synthesis with hardware description language, impact of logic synthesis, synthesis design flow, RTL description, technology mapping and optimization, technology library, design constraints Introduction to System Verilog, verification techniques.
SUGGESTED READING: 1. Peter J Ashenden, “The Designer’s Guide to VHDL,” Morgan Kaufmann Publishers. 2. Stefan Sjoholm & Lennart Lindth, “VHDL for Designers,” Prentice Hall. 3. J. Bhaskar, "Verilog HDL Synthesis - A Practical Primer,” Star Galaxy Publishing. 4. S. Palnitkar, "Verilog HDL: A Guide to Digital Design and Synthesis,” Prentice Hall. 5. Mintz**,** Mike, Ekendahl**,** Robert, “Hardware Verification with System Verilog: An Object-Oriented Framework,” Springer.

Course Code	Course Name	Course Structure	Pre-Requisite
ESD08	Optimization Techniques	L - T - P 3 - 1/0 - 0/2	_____
COURSE OUTCOME (CO): CO-1: To analyze various design parameters and the constraints involved with their efficient designing in analog circuits. CO-2: To develop ability to understand and compare various available optimization techniques CO-3: To develop ability to formulate mathematical models for these optimization techniques CO-4: To implement these mathematical models using softwares.			
COURSE CONTENT: Statistical modeling, sources of variations, Monte Carlo techniques, Process variation modeling-Pelgrom’s model, Principal component based modeling, Quad tree based modeling, Performance modeling-Response surface methodology, delay modeling, interconnect delay models, Statistical timing analysis, parameter space techniques, Bayesian networks Leakage models, High level statistical analysis, Gate level statistical analysis, dynamic power, leakage power, temperature and power supply variations,			

SCHEME OF COURSES – M.TECH. (EMBEDDED SYSTEMS AND VLSI)

High level yield estimation and gate level yield estimation.

Convex optimization**,** Convex sets, convex functions, geometric programming, trade-off and sensitivity analysis, Generalized geometric programming, geometric programming applied to digital circuit gate sizing, Floor planning, wire sizing, Approximation and fitting- Monomial fitting, Maxmonomial fitting, Posynomial fitting.

Genetic algorithm introduction, GA Technology-Steady State Algorithm-Fitness Scaling-Inversion GA for VLSI Design, Layout and Test automation- partitioning-automatic placement,routingtechnology,Mapping for FPGA- Automatic test generation- Partitioning algorithm Taxonomy-Multiway Partitioning Hybrid genetic-encoding-local improvement-WDFRComparison of Cas-Standard cell placement-GASP algorithm-unified algorithm GA routing procedures and power estimation, Global routing-FPGA technology mapping-circuit generation-test generation in a GA frame work-test generation procedures, Power estimation-application of GA-Standard cell placement-GA for ATG-problem encoding- fitness function-GA vs Conventional algorithm.

SUGGESTED READING:

1. Ashish Srivastava, Dennis Sylvester, David Blaauw “Statistical Analysis and Optimization for VLSI: Timing and Power,” Springer.

2. PinakiMazumder, E.Mrudnick, “Genetic Algorithm for VLSI Design,Layout and test Automation,” Prentice Hall.

3. Stephen Boyd, LievenVandenberghe “Convex Optimization”, Cambridge University Press.

4. BehzadRazavi, “Design of Analog CMOS Integrated Circuit,” Tata McGraw Hill.

Course Code	Course Name	Course Structure	Pre-Requisite
ESD09	Embedded Networking	L - T - P 3 - 1/0 - 0/2	SPC 001

COURSE OUTCOME (CO):

CO 1: To understand the fundamentals of different network types and topologies.

CO 2: To develop understanding of power-aware protocols for networks of small devices

CO 3: To explore newly established standards for embedded systems and ubiquitous computing

CO 4: To understand various techniques of wireless embedded networking and its applications

COURSE CONTENT:

Embedded Communication Protocols: Embedded Networking: Introduction – Serial/Parallel Communication – Serial communication protocols -RS232 standard – RS485 – Synchronous Serial Protocols -Serial Peripheral Interface (SPI) – Inter Integrated Circuits (I2C) – PC Parallel port programming - ISA/PCI Bus protocols –Firewire.

USB and CAN Bus: USB bus – Introduction – Speed Identification on the bus – USB States – USB bus communication: Packets –Data flow types –Enumeration –Descriptors –PIC 18 Microcontroller USB Interface – C Programs –CAN Bus – Introduction - Frames –Bit stuffing –Types of errors –Nominal Bit Timing–PIC microcontroller CAN Interface –A simple application with CAN.

Ethernet Basics: Elements of a network – Inside Ethernet – Building a Network: Hardware options –

SCHEME OF COURSES – M.TECH. (EMBEDDED SYSTEMS AND VLSI)

Cables, Connections and network speed – Design choices: Selecting components –Ethernet Controllers – Using the internet in local and internet communications – Inside the Internet protocol.
Embedded Ethernet: Exchanging messages using UDP and TCP – Serving web pages with Dynamic Data – Serving web pages that respond to user Input – Email for Embedded Systems – Using FTP – Keeping Devices and Network secure.
Wireless Embedded Networking: Wireless sensor networks – Introduction – Applications – Network Topology – Localization –Time Synchronization - Energy efficient MAC protocols –SMAC – Energy efficient and robust routing–Data Centric routing.

SUGGESTED READING:

1. Frank Vahid, Tony Givargis, "Embedded Systems Design: A Unified Hardware/Software Introduction," John & Wiley Publications.
2. Jan Axelson, "Parallel Port Complete: Programming, interfacing and using the PCs parallel printer port," Penram Publications.
3. Bhaskar Krishnamachari, "Networking Wireless Sensors," Cambridge Press.

Course Code	Course Name	Course Structure	Pre-Requisite
ESD10	Sensors and Actuators	L - T - P 3 - 1/0 - 0/2	SPC 002

COURSE OUTCOME (CO):

CO 1: Interpret physical principles applied in sensors and actuators
CO 2: To model and design sensors with desired physical and chemical properties
CO 3: Identify various types of sensors including thermal, mechanical, electrical, electromechanical and optical sensors
CO 3: To implement sensors for physical, chemical, and biochemical applications

COURSE CONTENT:

Sensors/Transducers: Principles – Classification – Parameters – Characteristics – Environmental Parameters (EP) – Characterization
Mechanical and Electromechanical Sensors: Introduction – Resistive Potentiometer – Strain Gauge – Resistance Strain Gauge – Semiconductor Strain Gauges -Inductive Sensors: Sensitivity and Linearity of the Sensor –Types-Capacitive Sensors:– Electrostatic Transducer– Force/Stress Sensors Using Quartz Resonators – Ultrasonic Sensors
Thermal Sensors: Introduction – Gas thermometric Sensors – Thermal Expansion Type Thermometric Sensors – Acoustic Temperature Sensor – Dielectric Constant and Refractive Index thermosensors – Helium Low Temperature Thermometer – Nuclear Thermometer – Magnetic Thermometer – Resistance Change Type Thermometric Sensors –Thermoemf Sensors– Junction Semiconductor Types– Thermal Radiation Sensors –Quartz Crystal Thermoelectric Sensors – NQR Thermometry – Spectroscopic Thermometry – Noise Thermometry – Heat Flux Sensors
Magnetic sensors: Introduction – Sensors and the Principles Behind – Magneto-resistive Sensors – Anisotropic Magnetoresistive Sensing – Semiconductor Magnetoresistors– Hall Effect and Sensors –

SCHEME OF COURSES – M.TECH. (EMBEDDED SYSTEMS AND VLSI)

Inductance and Eddy Current Sensors– Angular/Rotary Movement Transducers – Synchros –Synchro-resolvers - Eddy Current Sensors – Electromagnetic Flowmeter – Switching Magnetic Sensors SQUID Sensors

Radiation Sensors: Introduction – Basic Characteristics – Types of Photosensistors/Photo detectors– X-ray and Nuclear Radiation Sensors– Fiber Optic Sensors

Electro analytical Sensors: Introduction – The Electrochemical Cell – The Cell Potential – Standard Hydrogen Electrode (SHE) – Liquid Junction and Other Potentials – Polarization – Concentration Polarization-– Reference Electrodes - Sensor Electrodes – Electro ceramics in Gas Media .

Smart Sensors: Introduction – Primary Sensors – Excitation – Amplification – Filters – Converters – Compensation– Information Coding/Processing - Data Communication – Standards for Smart Sensor Interface – The Automation

Sensors –Applications: Introduction – On-board Automobile Sensors (Automotive Sensors)– Home Appliance Sensors – Aerospace Sensors –– Sensors for Manufacturing –Sensors for environmental Monitoring

Actuators: Pneumatic and Hydraulic Actuation Systems- Actuation systems – Pneumatic and hydraulic systems - Directional Control valves – Presure control valves – Cylinders - Servo and proportional control valves – Process control valves – Rotary actuators Mechanical Actuation Systems- Types of motion – Kinematic chains – Cams – Gears – Ratchet and pawl – Belt and chain drives – Bearings – Mechanical aspects of motor selection Electrical Actuation Systems-Electrical systems -Mechanical switches – Solid-state switches Solenoids – D.C. Motors – A.C. motors – Stepper motors

SUGGESTED READING:

1. D. Patranabis, “Sensors and Transducers,” Prentice Hall of India Learning Private Limited.
2. W. Bolton, “Mechatronics,” Pearson Education Limited.
3. D. Patranabis, “Sensors and Actuators,” Prentice Hall of India.

Course Code	Course Name	Course Structure	Pre-Requisite
ESD11	Hardware Software Co-design	L - T - P 3 - 1/0 - 0/2	SPC 002

COURSE OUTCOME (CO):

CO 1: To provide knowledge of hardware/software computing systems co-design techniques including behavioral modeling of both hardware and software components

CO 2: To understand their interaction, partitioning algorithms, analyzing and profiling techniques, simulation, synthesis, and verification of designed systems.

CO 3: To understand the complexity involved to partition the modern embedded system into software and hardware components, using an architecture strategy that will optimize performance, power consumption, development time, and cost.

COURSE CONTENT:

SCHEME OF COURSES – M.TECH. (EMBEDDED SYSTEMS AND VLSI)

Co- Design Issues: Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.
Co-Synthesis Algorithms: Hardware software synthesis algorithms: hardware – software partitioning distributed system cosynthesis.
Prototyping and Emulation: Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure
Target Architectures: Architecture Specialization techniques, System Communication infrastructure, Target Architectureand Application System classes, Architecture for control dominated systems (8051-Architectures forHigh performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.
Compilation Techniques and Tools for Embedded Processor Architectures: Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.
Design Specification and Verification: Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification
Languages for System – Level Specification and Design-I: System – level specification, design representation for system level synthesis, system level specification languages, Languages for System – Level Specification and Design-II: Heterogeneous specifications and multi language co-simulation, the cosyma system and lycos system.

SUGGESTED READING:

1. Jorgen Staunstrup, Wayne Wolf , “Hardware / Software Co- Design Principles and Practice,” Springer.
2. Giovanni De Micheli, Mariagiovanna Sami, “Hardware / Software Co- Design,” Kluwer Academic Publishers
3. Patrick R. Schaumont, “A Practical Introduction to Hardware/Software Co-design,” Springer.

Course Code	Course Name	Course Structure	Pre-Requisite
ESD12	Modern Analog Filter Design	L - T - P 3 - 1/0 - 0/2	SPC 001

COURSE OUTCOME (CO):

CO 1: To familiarize the students with the design methods of the analogue electrical filters.
CO 2: To analyze their operation and behavior in various analog integrated circuits.
CO 3: Ability to synthesize passive and active filters.
CO 4: To understand various modern high frequency filter designing techniques.
CO 5: To develop the ability to implement the filter circuits using computer aided design by PSpice and other software.

COURSE CONTENT:

Monolithic filters, digital filters, analog discrete-time filters, analog continuous-time filters, Introduction to analog filters, CMOS filters descriptive terminology, filter transmission, types and specifications, Filter

SCHEME OF COURSES – M.TECH. (EMBEDDED SYSTEMS AND VLSI)

transfer function, relationship among the time domain, frequency domain, s domain Active and passive filter synthesis. Standard low-pass approximations, Butterworth, Chebyshev, Inverse Chebyshev, Cauer, Bessel, Elliptical, frequency transformations, First-order and Second order filter functions, Active filters, inductor based filter, two integrator loop topology Switched capacitor filters, Basic principle and practical circuits, continuous type filters MOSFET-C, OTA-C filters, implementation techniques towards low power supply voltages and low distortion Filter synthesis for very high frequencies, synthesis methods, biquads, gyrators, Generalized immittance converter (GIC), inductor simulation using GIC, Analog filters in nanometer CMOS
SUGGESTED READING: 1. M. E. Van Valkenburg and Mac Elwyn Van Valkenburg, "Analog Filter Design," Oxford University Press. 2. Lawrence P. Huelsman, "Active and passive analog filter design: An introduction, Volume 1" McGraw-Hill Ryerson, Limited. 3. Larry D. Paarmann, "Design and Analysis of Analog Filters: A Signal Processing Perspective," Kluwer Academic Publishers.

Course Code	Course Name	Course Structure	Pre-Requisite
ESD13	Deep Sub Micron CMOS ICs	L - T - P 3 - 1/0 - 0/2	SPC 002
COURSE OUTCOME (CO): CO-1: Apply the circuit models to investigate CMOS circuits. CO-2: Able to design moderately sized CMOS circuits/ sub-systems and compute timing, power and parasitic forvarious CMOS Logic structures. CO-3: Able to evaluate various micron, deep sub micron and nanometer-scale technologies. CO-4: To understand the parasitic elements introduced by the deep submicron process.			
COURSE CONTENT: MOS scaling, classification, DSM (Deep submicron) effects on devices, physical and geometrical effects on the behavior of MOS transistor, carrier mobility, channel length modulation, short channel, narrow channel effects, drain feedback, hot carrier effects MOS transistor leakage mechanisms, weak inversion behavior, gate oxide tunneling, reverse-bias junction leakage, gate induced drain leakage, Impact ionization, overall leakage interactions and considerations Signal integrity, cross talk and signal propagation, power integrity, supply and ground bounce, substrate bounce, EMC, soft errors, Variability, spatial and time based variations, global and local variations, transistor matching, parameter, process corners, causes for variations Deep submicron IC reliability, punch through, electromigration, hot carrier degradation, negative bias temperature instability, Latch-up, Electro-static discharge, charge injection during fabrication process, Effects of scaling on MOS IC design and consequences for the technology roadmap for Semiconductors			
SUGGESTED READING:			

SCHEME OF COURSES – M.TECH. (EMBEDDED SYSTEMS AND VLSI)

1. Harry Veendrick, "Deep-Submicron CMOS ICs," Kluwer Academic publishers.
2. John Paul Uyemura, "Chip Design for Submicron VLSI," Thomson/Nelson.
3. Wolfgang nebel and Jean mermet, "Low power design in deep submicron electronics," NATO ASI series, Kluwer Academic Publishers.

Course Code	Course Name	Course Structure	Pre-Requisite
ESD14	ASIC Design	L - T - P 3 - 1/0 - 0/2	SPC 002

COURSE OUTCOME (CO):

CO-1: To understand the difference between, ASIC, full-custom and semi-custom design flows.
CO-2: To study about the implementation of automated design methodologies.
CO-3: To develop in-depth understanding of the ASIC design flow and role of standard cell libraries.
CO-4: To provide a comprehensive coverage of CAD algorithms used in the ASIC design flow.

COURSE CONTENT:

Introduction to ASICs, CMOS Logic, ASIC library design, types of ASICs, design flow, CMOS transistors, CMOS design rules, Combinational logic cell, Sequential logic cell, Data path logic cell, Transistors as resistors, Transistor parasitic capacitance, Logical effort, Library cell design, Library architecture

Programmable Asics, logic cells and I/O cells, Anti fuse, static RAM, EPROM, EEPROM technology, PREP benchmarks, Actel ACT , Xilinx LCA, Altera FLEX, Altera MAX, DC & AC inputs and outputs, Clock & power inputs, Xilinx I/O blocks

Programmable ASIC Interconnect, design software and low level design entry, Actel ACT, Xilinx LCA, Xilinx EPLD, Altera MAX 5000 and 7000, Altera MAX 9000, Altera FLEX, design systems, Logic synthesis, Half gate ASIC, Schematic entry, Low level design language, PLA tools, EDIF, CFI design representation

ASIC construction, Floor planning, Placement and routing, system partition, FPGA partitioning, partitioning methods, floor planning, placement, physical design flow, global routing, detailed routing, special routing, circuit extraction, DRC

SUGGESTED READING:

1. M.J.S. Smith, "Application - Specific Integrated Circuits," Addison Wesley Longman Inc.
2. Keith Barr, "ASIC Design in the Silicon Sandbox: A Complete Guide to Building Mixed-Signal Integrated Circuits," McGraw Hill.
3. Himanshu Bhatnagar, "Advanced ASIC Chip Synthesis," Kluwer Academic publishers.

Course Code	Course Name	Course Structure	Pre-Requisite
ESD15	Design of Semiconductor Memories	L - T - P 3 - 1/0 - 0/2	SPD 002

COURSE OUTCOME (CO):

SCHEME OF COURSES – M.TECH. (EMBEDDED SYSTEMS AND VLSI)

CO-1: To understand the circuit level operation of memories. CO-2: To develop strong understanding NVMs and flash memories. CO-3: To get familiar with the reliability issues in memory design CO-4: To acquire knowledge about FRAMs, analog memories and high density memory packaging.
COURSE CONTENT: MOS RAM technologies, SRAMs, architecture, SRAM cell and peripheral, Circuit operation, SRAM Technologies, SOI Technology, advanced SRAM architectures and technologies, DRAM technology development, CMOS DRAMs cell, theory and advanced cell structures Nonvolatile memories, MOS ROMs, PROMs, EPROMs, One-Time Programmable EPROMS, Electrically erasable PROMs, EEPROM technology and architecture, Nonvolatile SRAM-Flash Memories, advanced Flash Memory architecture Memory failure modes, reliability modeling, Prediction design for reliability, reliability test structures, reliability screening and qualification, radiation effects, radiation hardening, process and techniques, Radiation hardened memory characteristics, soft errors Ferroelectric random access memories (FRAMs), Gallium arsenide FRAMs, Analog memories, Magneto resistive RAMs, Experimental memory devices, Memory hybrids and MCMs (2D), Memory stacks and MCMs(3D), memory cards, high density memory packaging
SUGGESTED READING: 1. Ashok K. Sharma, “Advanced Semiconductor Memories: Architectures, Designs, and Applications,” John Wiley & Sons. 2. A.K Sharma, “Semiconductor Memories Technology, Testing and Reliability,” IEEE Press. 3. Luecke Mize Care, “Semiconductor Memory design & application,” Mc-Graw Hill.

Course Code	Course Name	Course Structure	Pre-Requisite
ESD16	Algorithms for VLSI Design Automation	L - T - P 3 - 1/0 - 0/2	_____
COURSE OUTCOME (CO): CO-1: To establish comprehensive understanding of the various phases of CAD for digital electronic systems CO-2: To develop strong understanding of IC design flow through CAD tools. CO-3: To study algorithms for automation from digital logic simulation to physical design, including test and verification. CO-4: To acquire knowledge and understanding of fundamental concepts in CAD and to establish capability for CAD tool development and enhancement.			
COURSE CONTENT: VLSI automation algorithms, General graph theory and basic VLSI algorithms, Partitioning, problem formulation, classification of partitioning algorithms, Group migration algorithms, simulated annealing & evolution, other partitioning algorithms Placement, floor planning & pin assignment, problem formulation, simulation base placement			

algorithms, other placement algorithms, constraint based floor planning, floor planning algorithms for mixed block & cell design, general & channel pin assignment Global Routing, problem formulation, classification of global routing algorithms, Maze routing algorithm, line probe algorithm, Steiner tree based algorithms, ILP based approaches, problem formulation, classification of routing algorithms, single layer routing algorithms, two layer channel routing algorithms, three layer channel routing algorithms and switchbox routing algorithms Over the cell routing & via minimization, two layers over the cell routers constrained & unconstrained via minimization, compaction, problem formulation, one-dimensional compaction, two dimension based compaction, hierarchical compaction.
SUGGESTED READING: 1. Sahib H.Gerez, "Algorithms for VLSI design automation," Wiley. 2. Naveed Shervani, "Algorithms for VLSI physical design Automation," Kluwer Academic Publisher. 3. Rolf Drechsheler : "Evolutionary Algorithm for VLSI," Springer. 5. Trimburger," Introduction to CAD for VLSI," Kluwer Academic publisher.

Course Code	Course Name	Course Structure	Pre-Requisite
ESD17	Low Power VLSI Design	L - T - P 3 - 1/0 - 0/2	_____
COURSE OUTCOME (CO): CO-1: To understand the basic analog and digital circuits suitable for low power design CO-2: To understand low power architectures CO-3: To understand the basic issues related to low power circuit design CO-4: To understand low power memory design CO-5: To understand the use of miscellaneous CAD tools			
COURSE CONTENT: Introduction, battery technology summary, sources of CMOS power consumption, need for low power VLSI chips, dynamic power, static power, switching power, computing power versus chip power, SOI and Bulk technology Impact of technology Scaling - Technology and Device, transistor sizing, gate oxide thickness, Technology options for low power, design options for power reduction, architectural level approaches, voltage scaling, power management, Circuit level approaches, Low power digital cells library Low power Analog integrated circuits, challenges in low voltage analog circuit design, issues about low power supply voltage. Basic building blocks in analog design, self cascode structure, flipped voltage follower Low voltage analog circuit design techniques, roadmap, design of analog circuits using low voltage implementation techniques such as Body bias, Bulk driven, FG			
SUGGESTED READING: 1. Gary K. Yeap, Farid N. Najm, "Low power VLSI design and technology," World Scientific Publishing Ltd. 2. Rabaey, Pedram, "Low power design methodologies," Kluwer Academic.			

SCHEME OF COURSES – M.TECH. (EMBEDDED SYSTEMS AND VLSI)

3. Kaushik Roy, SharatPrasad,"Low-Power CMOS VLSI Circuit Design," Wiley.
4. Christian Piguet, "Low-power CMOS circuits: technology, logic design and CAD tools," CRC Press, Taylor & Francis Group.

Course Code	Course Name	Course Structure	Pre-Requisite
ESD18	Neural networks in embedded applications	L - T - P 3 - 1/0 - 0/2	____

COURSE OUTCOME (CO):
CO 1: To understand the role of neural networks in engineering, artificial intelligence, cognitive modeling and embedded circuits.
CO 2: To provide knowledge of supervised learning in neural networks.
CO 3: To provide knowledge of computation and dynamical systems using neural networks.
CO 4: To provide knowledge of reinforcement learning and unsupervised learning using neural networks.

COURSE CONTENT:
Introduction to artificial neural networks, Fundamental models of artificial neural network, Perceptron networks, Feed forward networks, Feedback networks, Radial basis function networks, Associative memory networks.
Self organizing feature map, Learning Vector Quantization, Adaptive resonance theory, Probabilistic neural networks, neocgnitron, Boltzmann Machine.
Optical neural networks, Simulated annealing, Support vector machines, Applications of neural network in Image processing, Introduction to Embedded systems, Characteristic.
Features and Applications of an embedded system, Introduction to embedded digital signal processor, Embedded system design and development cycle, ANN application in digital camera, Implementation of Radial Basis Function, Neural Network on embedded system: real time face tracking and identity verification, Overview of design of ANN based sensing logic and implementation for fully automatic washing machine.

SUGGESTED READING:
1. S N Sivanandam, S Sumathi, S N Deepa, "Introduction to Neural Networks Using Matlab 6.0," Tata McGraw Hill Publication .
2. Simon Haykin, "Neural Networks: Comprehensive foundation," Prentice Hall Publication.
3. Frank Vahid, TonyGivargis, "Embedded System Design A unified Hardware/ Software Introduction," Wiley India Pvt. Ltd.
4. Rajkamal, "Embedded Systems Architecture, Programming and Design," Tata McGraw-Hill .

Course Code	Course Name	Course Structure	Pre-Requisite
ESD19	Internet of Things	L - T - P 3 - 1/0 - 0/2	SPC 003, SPD 015

COURSE OUTCOME (CO):

SCHEME OF COURSES – M.TECH. (EMBEDDED SYSTEMS AND VLSI)

CO 1: To understand the concept and application of internet of things in modern world. CO 2: To understand the architectural requirements of internet of things CO 3: Analyze various protocols involved and wireless vs. wired communication CO 4: To understand the various aspects/attributes involved like dependability, security, maintainability etc.
COURSE CONTENT: Industry domains: IoT in Sports, IoT in Cities/Transportation, IoT in the Home, IoT in Retail, IoT in Healthcare. Platforms: Hardware, SoC, sensors, device drivers, IoT standards, Cloud computing for IoT, Bluetooth, Bluetooth Low Energy, beacons. Protocols: NFC, RFID, Zigbee, MIPI, M-PHY, UniPro, SPMI, SPI, M-PCIe, Wired vs. Wireless communication, GSM, CDMA, LTE, GPRS, small cell. Services/Attributes: Big-Data Analytics and Visualization, Dependability, Security, Maintainability.
SUGGESTED READING: 1. Adrian McEwen, Hakim Cassimally, "Designing the Internet of Things," Wiley. 2. Dieter Uckelmann, Mark Harrison, Florian Michahelles , "Architecting the Internet of Things," Springer. 3. Sergei Evdokimov, Benjamin Fabian, Oliver Gunther, "RFID and the Internet of Things: Technology, Applications, and Security Challenges," Now Publishers.

Course Code	Course Name	Course Structure	Pre-Requisite
ESD20	Current Mode Techniques for Signal Processing	L - T - P 3 - 1/0 - 0/2	SPC 003
COURSE OUTCOME (CO): CO 1: To understand voltage and current mode architectures used in analog signal processing. CO 2: To design circuits capable of performing low power analog computation and processing of signals in CMOS. CO 3: Describe circuit techniques which allow efficient computation and signal processing in CMOS such as log-domain, switched capacitor correlated double sampling and spike domain.			
COURSE CONTENT: Current mode circuits from a translinear viewpoint, various translinear circuits-squaring, rms to DC conversion, square-rooting, geometric mean vector magnitude, multiplier/divider cells and trigonometric function generators, current-mode analog amplifiers, current followers, current conveyers, current feedback amplifiers and current mode op-amp architectures, High frequency CMOS transconductors Ga analog IC design, basic building blocks, current mode A/D, D/A converters, application of current feedback to voltage amplifiers, Current mode circuits for neural systems, current mode analog interface circuits for VLSI.			
SUGGESTED READING:			

SCHEME OF COURSES – M.TECH. (EMBEDDED SYSTEMS AND VLSI)

1. Chris Toumazou, F. J. Lidgey, David Haigh., "Analogue IC Design: The Current-mode Approach," IET.
2. Fei Yuan, "CMOS Current-Mode Circuits for Data Communications," Springer.
3. Technology Chris Toumazou, John B. Hughes, "Switched-currents: An Analogue Technique for Digital Technology," IET.

Course Code	Course Name	Course Structure	Pre-Requisite
ESD21	System on Chip Design	L - T - P 3 - 1/0 - 0/2	SPC 003, SPD 013

COURSE OUTCOME (CO):

CO-1: To analyze the functional and nonfunctional performance of the system early in the design process to support design decisions.

CO-2: To analyze hardware/software tradeoffs, algorithms, and architectures to optimize the system based on requirements and implementation constraints.

CO-3: Describe examples of applications and systems developed using a co-design approach.

CO-4: To appreciate issues in system-on-a-chip design associated with co-design, such as intellectual property, reuse, and verification.

COURSE CONTENT:

System-level and SoC design methodologies and tools; HW/SW Co-design: analysis, partitioning, real-time scheduling, hardware acceleration; Virtual platform models, co-simulation and FPGAs for prototyping of HW/SW systems; Transaction-Level Modeling (TLM) and Electronic System-Level (ESL) languages: System C; High-Level Synthesis (HLS): allocation, scheduling, binding, resource sharing, pipelining; SoC and IP integration, verification and test.

SUGGESTED READING:

1. Black, J. Donovan, "System C: From the Ground Up," Springer.
2. P. Marwedel, "Embedded System Design," Springer.
3. G. De Micheli, "Synthesis and Optimization of Digital Circuits," McGraw-Hill.
4. R. Zurawski (Editor), "Embedded Systems Handbook," CRC Press.
5. B. Eckel, "Thinking in C++," Prentice Hall.

Course Code	Course Name	Course Structure	Pre-Requisite
ESD22	Scripting Languages for Design Automation	L - T - P 3 - 1/0 - 0/2	_____

COURSE OUTCOME (CO):

CO-1: To develop basic understanding for the need of automation using scripting languages.

CO-2: To develop programming ability in Tcl.

CO-3: To develop programming ability in Perl.

CO-4: Introduction to basics of Object oriented programming concepts and basics of Python.

SCHEME OF COURSES – M.TECH. (EMBEDDED SYSTEMS AND VLSI)

COURSE CONTENT:

Introduction to Scripts and Scripting: Characteristics and uses of scripting languages, Introduction to PERL, Names and values, Variables and assignment, Scalar expressions, Control structures, Built-in functions, Collections of Data, Working with arrays, Lists and hashes, Simple input and output, Strings, Patterns and regular expressions, Subroutines, Scripts with arguments.

Advanced PERL: Finer points of Looping, Subroutines, Using Pack and Unpack, Working with files, Navigating the file system, Type globs, Eval, References, Data structures, Packages, Libraries and modules, Objects, Objects and modules in action, Tied variables, Interfacing to the operating systems, Security issues.

TCL: The TCL phenomena, Philosophy, Structure, Syntax, Parser, Variables and data in TCL, Control flow, Data structures, Simple input/output, Procedures, Working with Strings, Patterns, Files and Pipes, Example code.

Advanced TCL: The eval, source, exec and up-level commands, Libraries and packages, Namespaces, Trapping errors, Event-driven programs, Making applications 'Internet-aware', 'Nuts-and-bolts' internet programming, Security issues, running untrusted code, The C interface.

TK and JavaScript: Visual tool kits, Fundamental concepts of TK, TK by example, Events and bindings, Geometry managers, PERL-TK. JavaScript – Object models, Design Philosophy, Versions of JavaScript, The Java Script core language, Basic concepts of Python. Object Oriented Programming Concepts (Qualitative Concepts Only): Objects, Classes, Encapsulation, Data Hierarchy.

SUGGESTED READING:

1. David Barron, “The World of Scripting Languages,” Wiley Student Edition.
2. Clif Flynt, “Tcl/Tk: A Developer's Guide,” Morgan Kaufmann Series.
3. John Ousterhout, “Tcl and the Tk Toolkit,” Kindel Edition.

Course Code	Course Name	Course Structure	Pre-Requisite
ESD23	Optimization of CMOS Integrated Circuits	L - T - P 3 - 1/0 - 0/2	SPC 002, SPC 003

COURSE OUTCOME (CO):

CO-1: To understand the timing and power constraints and tradeoffs in digital CMOS Integrated circuits.
CO-2: To understand the gain and bandwidth related constraints and tradeoffs in analog CMOS integrated circuits.
CO-3: To determine the upper bounds on transistor sizes for optimization using relevant techniques for both digital and analog CMOS integrated circuits.
CO-4: To apply different algorithms for optimization of digital, analog and mixed signal blocks to achieve target specifications.

COURSE CONTENT:

Introduction to basic digital and analog CMOS integrated circuits such as transistor level realization of

SCHEME OF COURSES – M.TECH. (EMBEDDED SYSTEMS AND VLSI)

combinational (multiplexers, decoders etc.) and sequential circuits (flip-flops, counters, shift registers etc.), op-amps, comparators etc.
Timing characterization of digital CMOS integrated circuits, measurement of propagation delays, setup time, hold time, clock-to-output delay, data-to-output delay, clock skew, clock jitter etc. Power characterization in CMOS circuits including dynamic and leakage power dissipation.
Optimizing delays in digital CMOS circuits using logical effort theory, concept of logical effort, electrical effort, stage effort, delay optimization of multistage circuits. Technology calibration- deriving the relationship between transistor width and gate capacitance at a given process node.
Tradeoffs and Optimization in Analog circuits, MOS design from weak through strong inversion, MOS design complexity compared to bipolar design, Bipolar transistor collector current and transconductance, MOS drain current and transconductance, MOS drain source conductance, Analog CMOS electronic design automation tools and design methods.
MOS performance versus drain current, inversion coefficient, and channel length, Advantages of selecting drain current, inversion coefficient, and channel length in analog CMOS design, Substrate factor and inversion coefficient, Temperature effects, sizing relationship, drain current and bias voltages, small signal parameters and intrinsic voltage gain, body effect transconductance and relationship to substrate factor, drain conductance, capacitances and bandwidth, noise,
Tradeoffs in MOS performance, and design of differential pairs and current mirrors,
Design of CMOS operational transconductance amplifiers optimized for DC, Balanced and AC Performance, Extending optimization methods to smaller geometry processes and future technologies.

SUGGESTED READING:

1. Jan M. Rabaey, Anantha Chandrakasan, and Borivoje Nikolic, “Digital Integrated Circuits,” Prentice-Hall.
2. N Weste and D. Harris, “CMOS VLSI Design: Circuits and Systems Perspective,” Addison Wesley.
3. David M. Binkley, “Tradeoffs and optimization in Analog CMOS Design,” Wiley.

Course Code	Course Name	Course Structure	Pre-Requisite
ESD24	Soft Computing Techniques	L - T - P 3 - 1/0 - 0/2	SPC 001

COURSE OUTCOME (CO):
CO 1: To understand computational techniques like Genetic/ Evolutionary algorithms, Artificial Neural Networks, Fuzzy Systems, Machine learning and probabilistic reasoning etc.
CO 2: To apply Genetic Algorithms and Artificial Neural Networks as computational tools to solve a variety of problems in various area of interest ranging from Optimization problems to Text Analytics.
CO 3: To explain the fuzzy set theory and apply derivative based and derivative free optimization
CO 4: To discuss the neural networks and supervised and unsupervised learning networks
CO 5: To develop their computational formulations.

COURSE CONTENT:
Characterizing Soft Computing approaches, Introduction to Genetic Algorithms, Genetic Operators and

SCHEME OF COURSES – M.TECH. (EMBEDDED SYSTEMS AND VLSI)

Parameters, Genetic Algorithms in Problem Solving, Theoretical Foundations of Genetic Algorithms, Implementation Issues.
Mathematical model of Neuron, Perceptron and MLP, Characterizing Neural Network Architectures, Learning in Artificial Neural Networks; Supervised, Unsupervised and Competitive Learning paradigms; Learning rules and Functions, Hebbian Learning, Associative Memories, Self Organizing Maps, Computing with Artificial Neural Networks, Applications of Artificial Neural Networks in text analytics.
Introduction to Fuzzy Sets, Operations on Fuzzy sets, Fuzzy Logic, Fuzzy Measures.

SUGGESTED READING:

1. M. Mitchell, "An Introduction to Genetic Algorithms," Prentice-Hall.
2. E. Goldberg, "Genetic Algorithms in Search, Optimization, and Machine Learning," Addison-Wesley.
3. S. V. Kartalopoulos, "Understanding Neural Networks and Fuzzy Logic: Basic Concepts and Applications," IEEE Press - PHI.

Course Code	Course Name	Course Structure	Pre-Requisite
ESD25	Mixed Signal IC Design	L - T - P 3 - 1/0 - 0/2	SPD 011

COURSE OUTCOME (CO):
CO 1: To design and perform analysis of fundamental building blocks and basic analog circuits.
CO 2: to introduce circuit design concepts for basic building blocks used in mixed-signal integrated circuit designs.
CO 3: To provide a foundation for more complicated and advanced circuit designs
CO 4: To handle both practical design and layout issues involved.

COURSE CONTENT:
Analog and discrete-time signal processing, analog integrated continuous-time and discrete-time filters, Analog continuous-time filters, passive and active filters, basics of analog discrete-time filters and Z-transform
Switched-capacitor filters, Nonidealities in switched-capacitor filters, switched capacitor filter architectures, switched capacitor filter applications, Basics of data converters, Successive approximation ADCs, Dual slope ADCs, Flash ADC, Pipeline ADC
Hybrid ADC structures, high resolution ADC, DAC, Mixed signal layout, Interconnects and data transmission, Voltage-mode signaling and data transmission, Current-mode signaling and data transmission.
Introduction to frequency synthesizers and synchronization, basics of PLL, Analog PLL, Digital PLL, Delay Locked Loop (DLL).

SUGGESTED READING:

SCHEME OF COURSES – M.TECH. (EMBEDDED SYSTEMS AND VLSI)

1. R. Jacob Baker, "CMOS mixed-signal circuit design", Wiley India.
2. BehadRazavi, "Design of analog CMOS integrated circuits", McGraw-Hill.
3. R. Jacob Baker, "CMOS circuit design, layout and simulation" IEEE press.

Course Code	Course Name	Course Structure	Pre-Requisite
ESD26	Design for testability	L - T - P 3 - 1/0 - 0/2	SPD 011

COURSE OUTCOME (CO):

CO-1: To understand types of faults and also to study about fault detection

CO-2: To understand the concepts of the test generation methods.

CO-3: To understand the fault diagnosis methods will learn testing and verification in VLSI design process

CO-4: To understand Automatic test pattern generation concepts for combinational and sequential circuits

CO 5: To perform memory test, defect screening, SOC testing etc

COURSE CONTENT:

Introduction to Testing: Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modeling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

Logic and Fault Simulation: Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation, ATPG.

Testability Measures: SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

Built-In Self-Test: The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per-Scan BIST Systems, Circular Self Test Path System, Memory BIST, Delay Fault BIST.

Boundary Scan Standard: Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.

SUGGESTED READING:

1. M.L. Bushnell, V. D. Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits," Kluwer Academic Publishers.
2. M. Abramovici, M.A.Breuer and A.D Friedman, "Digital Systems and Testable Design," Jaico Publishing House.
3. P.K. Lala, "Digital Circuits Testing and Testability," Academic Press.

SCHEME OF COURSES – M.TECH. (EMBEDDED SYSTEMS AND VLSI)

SYLLABUS OF OPEN ELECTIVE COURSES

Course Code	Course Name	Course Structure	Pre-Requisite
EO001	Technical Communication	L-T-P 3-1-0	____

COURSE OUTCOME (CO):

CO-1: The course will improve writing and documentation skills of students with emphasis on the importance of effective communication with focus on choice of words, formation of proper sentence structures and writing styles.

CO-2: This will enhance the students capability to prepare technical documents and correspondence.

CO-3: The course will equip the student with good communications skills for placements, preparing SOPs and CVs.

CO-4: The course will sensitize the students towards research ethics, copyright and plagiarism.

COURSE CONTENT:

Definition of communication, meaning, importance & process of communication, objectives, types, C's of communication, barriers to communication human & non -human communication, distinctive features of human languages Business correspondence-definition, meaning and importance of business communication, business letters- purchase, enquiry, quotation, order, followup, acceptance-refusal Emphasis on (i) paragraph writing, its kinds, coherence & cohesion (ii)writing a paragraph/thesis: selection of topic and its development (iii) writing reports, manuals, notices, memos, agendas, minutes (iv)Interviews, speeches, presentations, Research ethics, methodologies, copyright, plagiarism

SUGGESTED READINGS:

1. Martin Hewing , "Advanced English Grammar: A Self Study Reference And Practice Book For Advanced South Asian Students," Cambridge University Press.

2. Meenakshi Raman & Sangeeta Sharma , "Technical Communication," Oxford University Press.

Course Code	Course Name	Course Structure	Pre-Requisite
EO002	Disaster Management	L-T-P 3-1-0	____

COURSE OUTCOME (CO):

CO-1: Demonstrate a critical understanding of key concepts in disaster risk reduction and humanitarian response.

CO-2: Critically evaluate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.

CO-3: Develop an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.

CO-4: Critically understand the strengths and weaknesses of disaster management approaches, planning

SCHEME OF COURSES – M.TECH. (EMBEDDED SYSTEMS AND VLSI)

and programming in different countries, particularly their home country or the countries they work in.
COURSE CONTENT: Disaster: Definition, Factors And Significance; Difference Between Hazard And Disaster; Natural And Manmade Disasters: Difference, Nature, Types And Magnitude. Repercussions Of Disasters And Hazards: Economic Damage, Loss Of Human And Animal Life, Destruction Of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts And Famines, Landslides And Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks And Spills, Outbreaks Of Disease And Epidemics, War And Conflicts. Study Of Seismic Zones; Areas Prone To Floods And Droughts, Landslides And Avalanches; Areas Prone To Cyclonic And Coastal Hazards With Special Reference To Tsunami; Post-Disaster Diseases And Epidemics Preparedness: Monitoring Of Phenomena Triggering A Disaster Or Hazard; Evaluation Of Risk: Application Of Remote Sensing, Data From Meteorological And Other Agencies, Media Reports: Governmental And Community Preparedness. Disaster Risk: Concept And Elements, Disaster Risk Reduction, Global And National Disaster Risk Situation. Techniques Of Risk Assessment, Global Co-Operation In Risk Assessment And Warning, People's Participation In Risk Assessment. Strategies for Survival. Meaning, Concept And Strategies Of Disaster Mitigation, Emerging Trends In Mitigation. Structural Mitigation And Non-Structural Mitigation, Programs Of Disaster Mitigation In India.
SUGGESTED READINGS: 1. R. Nishith, Singh AK, "Disaster Management in India: Perspectives, Issues and Strategies, " New Royal book Company. 2. Sahni, Pardeep Et.Al., "Disaster Mitigation Experiences And Reflections," Prentice-Hall.

Course Code	Course Name	Course Structure	Pre-Requisite
EO003	Basics of Financial Management	L-T-P 3-1-0	____
COURSE OUTCOME (CO): The course's objective is to provide a theoretical framework for considering corporate finance problems and issues and to apply these concepts in practice. In this course, you will enhance your knowledge and understanding of financial management. You will learn how managers should organize their financial transactions effectively and with integrity and how to give everybody the ability and confidence to tackle common financial problems in practice. It will also provide adequate preparation for future finance classes.			
COURSE CONTENT:			

SCHEME OF COURSES – M.TECH. (EMBEDDED SYSTEMS AND VLSI)

Nature, scope and objectives of financial management, Time value of money, Risk and return (including Capital Asset Pricing Model).

Long term investment decisions: The Capital Budgeting Process, Cash Flow Estimation, Payback Period Method, Accounting Rate of Return, Net Present Value (NPV), Net Terminal Value, Internal Rate of Return (IRR), Profitability Index.

Financing Decisions: Sources of long-term financing, Estimation of components of cost of capital, Methods for calculating Cost of Equity, Cost of Retained Earnings, Cost of Debt and Cost of Preference Capital, Weighted Average Cost of Capital (WACC). Capital Structure- Theories of Capital Structure (Net Income, Net Operating Income, MM Hypothesis, Traditional Approach). Operating and Financial leverage. Determinants of capital structure

Dividend Decisions: Theories for Relevance and irrelevance of dividend decision for corporate valuation- Walter's Model, Gordon's Model, MM Approach, Cash and stock dividends. Dividend policies in practice.

Working Capital Decisions: Concepts of Working Capital, Operating & Cash Cycles, sources of short term finance, working capital estimation, cash management, receivables management, inventory management.

SUGGESTED READINGS:

1. Khan, M.Y. and P.K. Jain, "Financial Management: Text and Problems," Tata McGraw Hill.
2. Srivastava, Rajiv, and Anil Mishra, "Financial Management," Oxford University Press, UK.
3. Chandra P., "Financial Management-Theory and Practice," Tata McGraw Hill.
4. Horne, Van; James C., John Wachowicz, "Fundamentals of Financial Management," Pearson Education.

Course Code	Course Name	Course Structure	Pre-Requisite
EO004	Basics of Human Resource Management	L-T-P 3-1-0	____

COURSE OUTCOME (CO): This course is designed to provide students with an understanding of human resource management (HRM) functions within organizations, including an appreciation of the roles of both HRM specialists and line managers in designing and implementing effective HRM policies and practices.

COURSE CONTENT:

Evolution and growth of human resource management (with special reference to scientific management and Human relations approaches). Role of HR in strategic management. Nature. objectives, scope, and functions of HR management.

Challenges of HR (the changing profile of the workforce - knowledge workers, employment opportunities in BPOs, IT and service industries, Flexi options), Workforce diversity (causes, paradox, resolution of diversity by management).

HRD; Human resource management as a profession. Concepts of line-staff in the structure of human resource department and the role of human resource manager.

SCHEME OF COURSES – M.TECH. (EMBEDDED SYSTEMS AND VLSI)

Manpower planning -objectives, elements, advantages, process. Job design - (simplification, rotation, enlargement, enrichment and approaches). Job analysis. Job evaluation. Recruitment (factors affecting, sources, policy, evaluation). Selection (procedure, tests, interviews). Placement and Induction.
SUGGESTED READINGS: 1. Aswathappa K., "Human Resource and Personnel Management," Tata McGraw-Hill. 2. Saiyadain S. Mirza, "Human Resource Management," Tata Mc-GrawHill.

Course Code	Course Name	Course Structure	Pre-Requisite
EO005	Project Management	L-T-P 3-1-0	____
COURSE OUTCOME (CO): In this comprehensive course, student will learn the fundamentals of project management: how to initiate, plan, and execute a project that meets objectives and satisfies stakeholders. This course provides a step-by-step guide to planning and executing a project and to develop a manageable project schedule.			
COURSE CONTENT: Objectives of Project Planning, monitoring and control of investment projects. Relevance of social cost benefit analysis, identification of investment opportunities. Pre-feasibility studies. Project Preparation: Technical feasibility, estimation of costs, demand analysis and commercial viability, risk analysis, collaboration arrangements; financial planning; Estimation of fund requirements, sources of funds. Loan syndication for the projects. Tax considerations in project preparation and the legal aspects. Project appraisal: Business criterion of growth, liquidity and profitability, social cost benefit analysis in public and private sectors, investment criterion and choice of techniques. Estimation of shadow prices and social discount rate. Project review/control-Evaluation of project.PERT/CPM. resource handling/leveling. Cost and Time Management issues in Project planning and management, success criteria and success factors, risk management.			
SUGGESTED READINGS: 1. Ravi Ravindran, "Operations Research and Management Science Handbook," CRC Press. 2. Harold Kerzner, "Applied Project Management: Best Practices on Implementation," John Wiley & Sons. 3. Goodpasture, J. C., "Quantitative Methods in Project Management, " J Ross Publishing. 4. Meredith, J. R. and Mantel Jr., S. J., "Project Management: A Managerial Approach," John Wiley.			

Course Code	Course Name	Course Structure	Pre-Requisite
EO006	Basics of Corporate Law	L-T-P	____

SCHEME OF COURSES – M.TECH. (EMBEDDED SYSTEMS AND VLSI)

		3-1-0	

COURSE OUTCOME (CO):
The objective of this Course is to provide in-depth knowledge of the Corporate laws and process related to integrate these aspects of management studies in decision making within an organization; analyze and interpret management information; make decisions based on the information available; communicate information effectively; understand and apply the theoretical aspects of accounting methods used for collecting, recording and reporting financial information; explain and appraise the taxation laws which govern corporations and individuals.

COURSE CONTENT:
Administration of Company Law, characteristics of a company; common seal; lifting of corporate veil; types of companies including private and public company, government company, foreign company, one person company, small company, associate company, dormant company, producer company; association not for profit; illegal association; formation of company, promoters and their legal position, pre incorporation contract and provisional contracts; on-line registration of a company.
Memorandum of association and its alteration, articles of association and its alteration, doctrine of constructive notice and indoor management, prospectus, shelf prospectus and red herring prospectus, misstatement in a prospectus; GDR; book building; issue, allotment and forfeiture of shares, calls on shares; public offer and private placement; issue of sweat capital; employee stock options; issue of bonus shares; transmission of shares, buyback and provisions regarding buyback; share certificate; D-Mat system; membership of a company.
Classification of directors, additional, alternate and adhoc director; women directors, independent director, small shareholders' director; director identity number (DIN); appointment, who can appoint a director, disqualifications, removal of directors; legal position, powers and duties; key managerial personnel, managing director, manager; meetings of shareholders and board; types of meeting, convening and conduct of meetings, requisites of a valid meeting; postal ballot, meeting through video conferencing, e-voting; committees of board of directors – audit committee, nomination and remuneration committee, stakeholders relationship committee, corporate social responsibility committee; prohibition of insider trading.

SUGGESTED READINGS:
1. Hicks, Andrew & Goo S.H., "Cases and Material on Company Law," Oxford University Press.
2. Gowar, LCB, "Principles of Modern Company Law," Stevens & Sons, London.
3. Hanningan Brenda, "Company Law," Oxford University Press.

Course Code	Course Name	Course Structure	Pre-Requisite
EO007	Biological Computing	L-T-P 3-1-0	____

COURSE OUTCOME (CO):
CO-1. To understand computing in context of biological systems
CO-2. To understand computing languages needed to solve biological problems

SCHEME OF COURSES – M.TECH. (EMBEDDED SYSTEMS AND VLSI)

CO-3. To acquire computational skills for analysis of biological processes through grid computing CO-4. To gain knowledge of different biological databases and their usage CO-5. To gain innovative insight into DNA computing
COURSE CONTENT: Introduction, Orientation and UNIX, Python: Introduction to Variables and Control flow, Python II - Parsing In and Output, Python III - Scripting and Functions, Python IV- Number Crunching and Plotting, Grid computing, Biogrid, R basics and Visualization, Unix for fast text processing, SQL Database Biological databases, R for speed, R for fun, Local BLAST, Unit Testing and Code Correctness DNA computing,
SUGGESTED READINGS: 1. H. Bolouri, R. Paton, "Computations in cells & tissues," Springer. 2. Haubold Bernhard and Wiehe Thomas, "Introduction to Computational Biology: An Evolutionary Approach," Springer.

Course Code	Course Name	Course Structure	Pre-Requisite
EO008	Sociology	L-T-P 3-1-0	____
COURSE OUTCOME (CO): Sociology is a major category of academic disciplines, concerned with society and the relationships among individuals within a society. It in turn has many branches, each of which is considered a "social science".			
COURSE CONTENT: The Development of Sociology in the 19th Century Science, scientific method and critique. Major theoretical strands of research methodology. Positivism and its critique. Fact value and objectivity. Non- positivist methodologies. Sociological theories of religion. Types of religious practices: animism, monism, pluralism, sects, cults. Religion in modern society: religion and science, secularization, religious revivalism, fundamentalism. Sociological theories of power. Power elite, bureaucracy, pressure groups, and political parties. Nation, state, citizenship, democracy, civil society, ideology. Protest, agitation, social movements, collective action, revolution. Kar l Marx- Historical materialism, mode of production, alienation, class struggle. Emile Durkheim- Division of labour, social fact, suicide, religion and society. Max Weber- Social action, ideal types, authority, bureaucracy, protestant ethic and the spirit of capitalism. Talcolt Parsons- Social system, pattern variables. Robert K. Merton- Latent and manifest functions, conformity and deviance, reference groups. Mead - Self and identity.			
SUGGESTED READINGS: 1. Beteille Andre, "Sociology: Essays in Approach and Method," Oxford University Press. 2. Giddens Anthony" Sociology," Polity Press. 3. Weber M. , "*The Methodology of the Social Sciences,"* New York: Free Press.			

SCHEME OF COURSES – M.TECH. (EMBEDDED SYSTEMS AND VLSI)

Course Code	Course Name	Course Structure	Pre-Requisite
EO009	Entrepreneurship	L-T-P 3-1-0	____
COURSE OUTCOME (CO): This Course Aims at Instituting Entrepreneurial skills in the students by giving an overview of who the entrepreneurs are and what competences are needed to become an entrepreneur.			
COURSE CONTENT: Concept and Definitions, Entrepreneur v/s Intrapreneur; Role of entrepreneurship in economic development; Entrepreneurship process; Factors impacting emergence of entrepreneurship; Managerial versus entrepreneurial Decision Making; Entrepreneur v/s Investors; Entrepreneurial attributes and characteristics; Entrepreneurs versus inventors; Entrepreneurial Culture; Women Entrepreneurs; Social Entrepreneurship; Classification and Types of Entrepreneurs; EDP Programmes; Entrepreneurial Training; Traits/Qualities of an Entrepreneurs. Generating Business idea- Sources of Innovation, methods of generating ideas, Creativity and Entrepreneurship; Challenges in managing innovation; Business planning process; Drawing business plan; Business plan failures; Entrepreneurial leadership- components of entrepreneurial leadership; Entrepreneurial Challenges; Legal issues – forming business entity, considerations and Criteria, requirements for formation of a Private/Public Limited Company, Intellectual Property Protection- Patents Trademarks and Copyrights – importance for startups, Legal Acts Governing Business in India. Marketing plan– for the new venture, environmental analysis, steps in preparing marketing plan, marketing mix, contingency planning; Organizational plan – designing organization structure and Systems; Financial plan – pro forma income statements, pro forma cash budget, funds Flow and Cash flow statements; Pro forma balance sheet; Break Even Analysis; Ratio Analysis. Debt or equity financing, Sources of Finance- Commercial banks, private placements, venture capital, financial institutions supporting entrepreneurs; Lease Financing; Funding opportunities for Startups in India. Managing growth and sustenance- growth norms; Factors for growth; Time management, Negotiations, Joint ventures, Mergers & acquisitions.			
SUGGESTED READINGS: 1. Kumar Arya, “Entrepreneurship: Creating and Leading an Entrepreneurial Organization,” Pearson. 2. Hishrich. Peters, “Entrepreneurship: Starting, Developing and Managing a New Enterprise,” Irwin. 3. Taneja, Entrepreneurship, Galgotia Publishers. 4. Barringer, Brace R., and R. Duane Ireland, “Entrepreneurship,” Pearson Prentice Hall.			

Course Code	Course Name	Course Structure	Pre-Requisite
EO010	Social Work	L-T-P 3-1-0	____

SCHEME OF COURSES – M.TECH. (EMBEDDED SYSTEMS AND VLSI)

COURSE OUTCOME (CO): In this course students will learn about various methods of social work, about community organization, social welfare administration, Problems pertaining to Marriage, Family and caste.

COURSE CONTENT:

Philosophy and Methods. Social work: Meaning, Objectives, Scope, Assumptions & Values; History of Social work in U.K. U.S.A. and India, philosophy of Social Work. Democratic (Equality, Justice Liberty & Fraternity) and Humanitarian (Human Rights) Matrix. Social works as a profession. Meaning, Scope Principles, Processes (Psychosocial study, Assessments, treatment-goal formulation and techniques), Evaluation, Follow-up and Rehabilitation. Social Groups work: Meaning, Objective, Principles, Skills, Processes (Study, Diagnosis, treatment and evaluation), Programme, Planning and Development, Role of Social group worker, Leadership Development. Meaning, Objective, Principles, Approaches, Roles of Community Organization Worker.
Meaning Scope, Auspices-Private and Public, Principles, Basic Administrative Processes and Practice decision making communication, planning. organisation, budgeting and finacial control, reporting. Social work Research: Meaning objectives, types, scope, scientific method, Selection and formulation of the problem Research Design Sampling, Sources and Methods of Data Collection, Processing of Data, analysing and interpretation, Report writing. Social Action: Meaning, Scope, approaches (Sarvodays, Antyodaya etc.) and Strategies. Dowry- child Marriage, Divorce, Families with working couples, Disorganised Families, Families with Emigrant Heads of the Households, Gender Inequality, Authoritarian Family structure, Major Changes in Caste systems and problem of casteism. Problems Pertaining of Weaker Sections. Problems of Children, Women Aged. Handicapped and Backward Classes (SCs, STs, and other Backward Classes). **Problems of Deviance:** Truancy Vagrancy and Juvenile Delinquency, Crime, White Colla Crime, Organized Crime, Collective Violence, Terrorism, Prostitution and Sex Related Crimes. Social Vices: Alcohilism. Drug Addiction, Beggary, Corruption and communalism. **Problems of Social Structure:** Poverty, Unemployment, Bonded Labour, Child Labour. **Fields of Soclal work India:** Child Development, Development of Youth, Women's Empowerment, Welfare of aged, Welfare of Physically. Mentally and Social Handicapped, Welfare of backward Classes (SCs, STs and Other Backward Classes) Rural Development Urban Community Development, Medical And Psychiatric Social work, Industrial Social work, Social Security offender

SCHEME OF COURSES – M.TECH. (EMBEDDED SYSTEMS AND VLSI)

Reforms.
SUGGESTED READINGS: 1. Rajni Bedi , "Social Work: An Introductory," Regal Publications. 2. Sanjay Bhattacharya , "Social Work: An Integrated Approach," Deep and Deep.

Course Code	Course Name	Course Structure	Pre-Requisite
EO011	Intellectual property and Patenting	L-T-P 3-1-0	____
COURSE OUTCOME (CO): The objective of this Course is to provide in-depth knowledge of the laws and process related to Trademarks, Copyrights and other forms of IPs with focus on Patents, the Indian and International Patent filing procedure, drafting patent application and conducting prior art searches. Students will be exposed to the technical, management and legal aspects of IP and Patents.			
COURSE CONTENT: Historical and philosophical background of patents and other intellectual property, Patent System: the Constitution, Congress, Patent Office (PTO), and courts; Analyzing and understanding judicial opinions Legal fundamentals of patent protection for useful inventions**,** Design and plant patents, Legal fundamentals of copyright protection, Similarity and access, Expression vs. ideas and information, merger, Fair use of copyrighted works (e.g., for classroom use), Contributory copyright infringement, Critical differences between patent and copyright protection, Copyright infringement distinguished from plagiarism, Legal fundamentals of trade-secret protection, Legal fundamentals of trademark protection New and useful: (A) The legal requirement of novelty (B) First to invent vs. first inventor to file, The legal requirement of non-obviousness. Anatomy of a patent application, Adequate disclosure, The art of drafting patent claims, Patent searching: (A) Purposes and techniques, Actions for patent infringement, Interpretation of claims, Doctrine of equivalents, Product testing as a possibly infringing use, Doctrine of exhaustion			
SUGGESTED READINGS: 1. Rines, Robert H., "Create or Perish: The Case for Inventions and Patents," Acropolis.			

Course Code	Course Name	Course Structure	Pre-Requisite
EO012	Supply Chain Management and Logistics	L-T-P 3-1-0	____
COURSE OUTCOME (CO): Supply chain management consists of all parties (including manufacturer, marketer, suppliers, transporters, warehouses, retailers and even customers) directly or indirectly involved in fulfillment of a customer. The main objective is to acquaint the students with the concepts and tools of supply chain management and logistics as relevant for a business firm.			

SCHEME OF COURSES – M.TECH. (EMBEDDED SYSTEMS AND VLSI)

COURSE CONTENT: Concept of supply chain management (SCM) and trade logistics; Scope of logistics; Logistic activities – an Overview; Contribution of logistics at macro and micro levels; SCM and trade logistics; Business view of SCM; Concept, span and process of integrated SCM; Demand management – methods of forecasting; Supply chain metrics (KPIs), performance measurement and continuous improvement; Product development Process and SCM; Strategic role of purchasing in the supply chain and total customer satisfaction; Types of purchases; Purchasing cycle. Role of Relationship marketing in SCM; Managing relationships with suppliers and customers; Captive buyers and suppliers; Strategic partnerships; Supplier-retailer collaboration and alliances. Transportation-Importance of effective transportation system; Service choices and their characteristics; inter-modal services; Transport cost characteristics and rate fixation; In-company management vs. out-sourcing; World sea borne trade; International shipping- characteristics and structure; Liner and tramp operations; Liner freighting; Chartering-Types, principles and practices; Development in sea transportation-Unitization, containerisation, inter and multimodal transport; CFC and ICD. Air transport: Set up for air transport and freight rates; Carriage of Goods by sea -Role and types of cargo intermediaries. Warehousing and inventory management: Reasons for warehousing; Warehousing evaluation and requirements; Warehousing location strategies; Inventory management principles and approaches; Inventory categories -EOQ, LT, ICC Technology in logistics – EDI, bar Coding, RFID etc., data warehousing, electronic payment transfers; Business management systems; TRADITIONAL ERP, SPECIAL ERP, MR, DRP, PDM, EIP, CPFR, WMS, TMS; Re-engineering the supply chain- Future directions. Party logistic outsourcing –challenges and future directions.
SUGGESTED READINGS: 1. Christopher, M., “Logistics and Supply Chain Management,” Prentice Hall. 2. Handfield and Nicholas, Jr., “Introduction to Supply Chain Management,” Prentice Hall. 3. Jhon J Coyle, C. Jhonand Langley,Brian J Gibs, “Logistics approach to Supply Chain Management,” Cengage Learning.

Course Code	Course Name	Course Structure	Pre-Requisite
EO013	Organization Development	L-T-P 3-1-0	____
COURSE OUTCOME (CO): Organisation Development is a growing field of Human Resource Management. It has its foundations in a number of behavioural and social sciences .			
COURSE CONTENT: Organizational Systems and Human Behavior - Developing a basic knowledge of how organizations and groups function as systems; introducing and discussing various theoretical approaches and issues. Interpersonal and Consulting Skills - Increasing effectiveness as a change agent by providing a variety of opportunities in order to increase self-awareness, practice alternative ways of approaching personal and			

SCHEME OF COURSES – M.TECH. (EMBEDDED SYSTEMS AND VLSI)

interpersonal problem-solving and develop basic consulting and interviewing skills. Introduction to Organization Development - Introducing some basic theories, models and methods in the field of organization development, especially those relating to the role of consultant and strategies for change. Intervention and Change in Organizations Consolidating and further developing consulting skills and strategies Action Research Project - Carrying out a change activity in an organization, while also researching the effects and for the process. This provides participants with an opportunity to consolidate and de, menstruate skills and knowledge gained in other units of the course
SUGGESTED READINGS: 1. Mee-Yan, Cheung-Judge, "Organization Development: A Practitioner's Guide for OD and HR," Koran Page.

Course Code	Course Name	Course Structure	Pre-Requisite
EO014	ndustrial organisation and managerial economics	L-T-P 3-1-0	____
COURSE OUTCOME (CO): This course helps students in understanding the basics of management and Industrial organisation.			
COURSE CONTENT: Principles of management, General idea, various functions, scope of engineering. Organisation structure, Types, merits and demerits. Plant location and layout, Factors effecting location, types of layout. Production planning and control, Sequence of planning and control of production. Scheduling, routing, dispatching. Methods Study, Methods analysis, time study methods of rating. General idea of personnel management, Industrial psychology, job evaluation and monitoring. Business decision making and forward planning. Demand and demand for casting of production analysis- prices and pricing decision-profit and capital, management. Analysis of inter-industry relation, macro-economics and business.			
SUGGESTED READINGS: 1. Koutsoyiannis A, " Modern Microeconomics," Palgrave Macmillan U.K.			

Course Code	Course Name	Course Structure	Pre-Requisite
EO015	Global Strategies and Technology	L-T-P 3-1-0	____
COURSE OUTCOME (CO): This subject focuses on the specifics of strategy and organization of the multinational company, and provides a framework for formulating successful and adaptive strategies in an increasingly complex world economy.			

SCHEME OF COURSES – M.TECH. (EMBEDDED SYSTEMS AND VLSI)

COURSE CONTENT: Globalization of industries, the continuing role of country factors in competition, organization of multinational enterprises, and building global networks, Analysis of competitive situations from the general management point of view, including fit between key environmental forces and the firm's resources, and changes in these over time. Formulating and implementing strategy based on that analysis. Developing and leveraging a firm's core competencies to gain long-term sustainable advantage.
SUGGESTED READINGS: 1. Mike W. Peng , "Global Strategy," South Western College Pub. 2. Pankaj Ghemawat, "Redefining Global Strategy," Harward Business Review Press.

Course Code	Course Name	Course Structure	Pre-Requisite
EO016	Engineering System Analysis and Design	L-T-P 3-1-0	____
COURSE OUTCOME (CO): The students will learn about system definitions and role of system analyst. They will learn about system modeling and design. They will be exposed to System Implementation and Maintenance issues.			
COURSE CONTENT: System definition and concepts: Characteristics and types of system, Manual and automated systems Real-life Business sub-systems: Production, Marketing, Personal, Material, finance Systems models types of models: Systems environment and boundaries, Real time and distributed systems, Basic principles of successful systems Systems analyst: Role and need of systems analyst, Qualifications and responsibilities, Systems Analyst, agent of change. Various phases of systems development life cycle: Analysis, Design, Development, Implementation, Maintenance Systems Design and modeling: Process modeling, Logical and physical design, Design representation, Systems flowcharts and structured charts, Data flow diagrams, Common diagramming conventions and guidelines using DFD and ERD diagrams. Data Modeling and systems analysis, designing the internals: Program and Process design, Designing Distributed Systems User Interfaces – Relational Analysis – Database design – program design– structure chart – HIPO – SSADM – Alternate Life cycles – Prototypes. System Implementation and Maintenance: Planning considerations, Conversion methods, producers and controls, System acceptance Criteria, System evaluation and performance, Testing and validation, Systems qualify Control and assurance, Maintenance activities and issues.			
SUGGESTED READINGS: 1. Harysz kiewycz, "Introduction to Systems Analysis and Design," Prentice Hall of India. 2. James A Senn, "Analysis and Design of Information Systems," McGraw Hill.			

SCHEME OF COURSES – M.TECH. (EMBEDDED SYSTEMS AND VLSI)

Course Code	Course Name	Course Structure	Pre-Requisite
EO017	Biology for Engineers	L-T-P 3-1-0	____
COURSE OUTCOME (CO): CO-1. General understanding of organization in biological systems CO-2. Conceptual knowledge of functioning in biological systems CO-3. Clarity about relevance of Biology to engineering graduates CO-4. Understanding human body or any other suitable organism as a study-model for engineering students. CO-5. Understanding electrical, chemical and magnetic forces, and communication networks in biosystem.			
COURSE CONTENT: The Biological system – An Introduction; Biomolecules &self assemblies; Molecular recognition; Bioenergetics; Communication network in biosystem; Mechanics in biology; Storage, preservation and propagation of biological information; Biomaterials in engineering applications; Organisms as factories for biomaterials; Engineering organisms for novel applications			
SUGGESTED READINGS: 1. T. Johnson , "Biology for Engineers," CRC Press. 2. Michael Small , "Dynamics of Biological System," CRC Press. 3. Johnny T. Ottesen, MS Olufsen, JK Larsen , "Applied Mathematical Models and Human Physiology," Society for Industrial and Applied Mathematics.			

Course Code	Course Name	Course Structure	Pre-Requisite
EO018	Energy Environment and Society	L-T-P 3-1-0	____
COURSE OUTCOME (CO): CO-1: To be able to assess the energy resources available worldwide CO-2: To understand the negative impact of conventional energy resource utilization on ecosystem CO-3: To learn about various types of pollutions and their control strategies CO-4: To understand renewable energy resources and their socio-economic impac			
COURSE CONTENT: Introduction to Environment, Energy and its impact on society Universe, Environment and Ecosystem: Origin of earth, atmosphere, Origin of Life, Ecosystem, Biotic and abiotic components, Ecological pyramids, Food chain, Food web, Habitat and Niche, Major ecosystems, Atmosphere, Biodiversity Pollution: Air Pollution, Water Pollution, Soil Pollution, Noise Pollution Energy: Different sources of			

SCHEME OF COURSES – M.TECH. (EMBEDDED SYSTEMS AND VLSI)

Energy, Renewable sources of energy, Non renewable energy, Bioenergy, Bioethanol and Biodiesel, Biofertilizers, Biopesticides and Biopolymers, Environmental Ethics and Morals.
SUGGESTED READINGS: 1. Kishore V V N, "Editor, Renewable Energy Engineering and Technology: Principles and Practice," The Energy and Resources Institute (TERI). 2. G. N. Tiwari and M. K. Ghosal, "Fundamentals of Renewable Energy Sources," Narosa Publishing House. 3. Mital K. M, "Biogas Systems: Principles and Applications," New Age International Publishers.

Course Code	Course Name	Course Structure	Pre-Requisite
EO019	Public Policy and Governance	L-T-P 3-1-0	____
COURSE OUTCOME (CO): Students will be introduced to Public Policy and Administrative governance. They will also learn about Administrative Governance.			
COURSE CONTENT: Introduction to Public Policy and Administrative Governance: Introduction to public policy, econometrics for policy research, policy analysis, economics for public decision making. Public Bureaucracy in Theory and Practice: Benefit cost analysis, public budgeting, revenue and expenditures, managing and leading public service organisations. Administrative Governance: The Challenge of Policy Implementation, public and non-profit programme evaluation. Non-state Actors in Policy-making and Administrative Governance: governance in twenty-first century, Social Diversity and the Question of "Difference" in Policy-making and administrative Governance			
SUGGESTED READINGS: 1. Beryl Radin, "Beyond Machiavelli: Policy Analysis Reaches Midlife," Georgetown University Press. 2. Frank R. Baumgartner, Jeffrey M. Berry, Marie Hojnacki, and David C. Kimball, "Lobbying and Policy Change: Who Wins, Who Loses, and Why. Chicago," University of Chicago Press. 3. Timothy Conlan, Paul Posner, and David Beam, "Pathways of Power: The dynamics of National Policymaking," Georgetown University Press.			