DIGITAL SIGNAL PROCESSING

DSE (Electronics) Sem V
(For Physics and Electronics as core subjects)

Course Title & Code	Credits	Credit distribution of the course			Eligibility Criteria	Pre-requisite of the course
		Lecture	Tutorial	Practical		
Digital Signal Processing Physics DSE 5	**4**	**2**	**0**	**2**	Class XII pass with Physics and Mathematics as main subjects	Basics of digital electronics and analog electronics

LEARNING OBJECTIVES

This paper describes the discrete-time signals and systems, Fourier transform representation of aperiodic discrete time signals. This paper also highlights the concept of filters and realization of digital filters. At the end of the syllabus, students will develop an understanding of discrete and fast Fourier transform.

LEARNING OUTCOMES

At the end of this course, students will be able to develop following learning outcomes.

- Students will learn basic discrete-time signal and system types, convolution sum, impulse and frequency response concepts for linear time-invariant (LTI) systems.
- The student will be in position to understand use of different transforms and analyse the discrete time signals and systems. They will learn to analyse a digital system using z- transforms and discrete time Fourier transforms, region of convergence concepts, their properties and perform simple transform calculations.
- The student will realize the use of LTI filters for filtering different real world signals. The concept of transfer Function and difference-equation system will be introduced. Also, they will learn to solve difference equations.
- Students will develop an ability to analyze DSP systems like linear-phase, FIR, IIR, All-pass, averaging and notch Filter etc.

- Students will be able to understand the discrete Fourier transform (DFT) and realize its implementation using FFT techniques.
- Students will be able to learn the realization of digital filters, their structures, along with their advantages and disadvantages. They will be able to design and understand different types of digital filters such as finite and infinite impulse response filters for various applications.

SYLLABUS OF PHYSICS DSE 5

THEORY **COMPONENT**

Unit – I **(7 Hours)**

Discrete-Time Signals and Systems: Classification of signals, transformations of the independent variable, periodic and aperiodic signals, energy and power signals, even and odd signals, discrete time systems, system properties, impulse response, convolution sum, graphical and analytical method, properties of convolution (general idea), sum property system response to periodic inputs, relationship between LTI system properties and the impulse response

Unit – II **(9 Hours)**

Discrete time Fourier transform: Fourier transform representation of aperiodic discrete time signals, periodicity of DTFT, properties; linearity; time shifting; frequency shifting; differencing in Time Domain; Differentiation in Frequency Domain; Convolution Property. The z-Transform: Bilateral (Two-Sided) z-Transform, Inverse z-Transform, Relationship Between z-Transform and Discrete-Time Fourier Transform, z-plane, Region-of-Convergence; Differentiation in the z-Domain; Power Series Expansion Method (General Idea). Transfer Function and Difference-Equation System.

Unit – III **(10 Hours)**

Filter Concepts: Phase Delay and Group delay, Zero-Phase Filter, Linear-Phase Filter, Simple FIR Digital Filters.Only Qualitative treatment
Discrete Fourier Transform: Frequency Domain Sampling (Sampling of DTFT), The Discrete Fourier Transform (DFT) and its Inverse, DFT as a Linear transformation, Properties; Periodicity; Linearity; Circular Time Shifting; Circular Frequency Shifting; Circular Time Reversal; Multiplication Property; Parseval's Relation (General Idea), Linear Convolution Using the DFT (Linear Convolution Using Circular Convolution).

Unit – IV **(4 Hours)**

Realization of Digital Filters: FIR Filter structures; Direct-Form; Cascade-Form Finite Impulse Response Digital Filter: Advantages and Disadvantages of Digital Filters, Types of Digital Filters: FIR Filters

References:

Essential Readings:

1) Digital Signal Processing, T. K. Rawat, 2015, Oxford University Press, India
2) Digital Signal Processing, S. K. Mitra, McGraw Hill, India. st
3) Principles of Signal Processing and Linear Systems, B. P. Lathi, 1 edition, 2009, Oxford University Press.

4) Fundamentals of signals and systems, P.D. Cha and J.I. Molinder, 2007, Cambridge University Press
5) Digital Signal Processing Principles Algorithm & Applications, J. G. Proakis and D. G. Manolakis, 4th edition, 2007, Prentice Hall.

Additional Readings: nd

1) Digital Signal Processing, A. Kumar
2) Digital Signal Processing, P. S. R. Diniz, E. A. B. da Silva and S. L. Netto, 2nd edition, 2017, Cambridge University Press

PRACTICAL COMPONENT

(15 Weeks with 4 hours of laboratory session per week)

- Introduction to numerical computation software Scilab/Matlab/Python be introduced in the lab.
- Sessions on the review of experimental data analysis, sources of error and their estimation in detail, writing of scientific laboratory reports including proper reporting of errors.
- Application to the specific experiments done in the lab"

<u>At least six experiments to be performed from the following using Scilab/ Matlab/ Python</u>

1) Write a program to generate and plot the following sequences:
   (a) Unit sample sequence $\delta(n)$,
   (b) unit step sequence *u(n)*, (c) ramp sequence *r(n)*, (d) real valued exponential sequence $x(n) = (0.8)^n u(n)$ for $0 \leq n \leq 50$.
2) Write a program to compute the convolution sum of a rectangle signal (or gate function) with itself for N = 5

$$x(n) = rec\left(\frac{n}{2N}\right) = \prod \left(\frac{n}{2N}\right) = \{1 - N \leq n \leq N) \ other\ wise$$

3) An LTI system is specified by the difference equation *y(n)=0.8y(n-1)+x(n)*
   (a) Determine $H(e^{iw})$
   (b) Calculate and plot the steady state response *y(n)* to $x(n) = cos\ cos\ (0.5\pi n)\ u(n)$
4) Given a casual system *y(n)=0.9y(n-1)+x(n)*
   a. Find H(z) and sketch its pole-zero plot
   b. Plot the frequency response $|H(e^{jw})|$ and $\angle H(e^{jw})$
5) Design a digital filter to eliminate the lower frequency sinusoid of *x(t)=sin7t+sin200t*. The sampling frequency is 500 Hz. Plot its pole zero diagram, magnitude response, input and output of the filter.
6) Let *x(n)* be a 4-point sequence:

$x(n) = \{1,1,1,1\} = \{1 \ \ 0 \leq n \leq 3\ 0 \ \ otherwise$

Compute the DTFT $X(e^{jjii})$ and plot its magnitude
   (a) Compute and plot the 4 point DFT of *x(n)*
   (b) Compute and plot the 8 point DFT of *x(n)* (by appending 4 zeros)

(c) Compute and plot the 16 point DFT of *x(n)* (by appending 12 zeros)

7) Let *x(n)* and *h(n)* be the two 4-point sequences,

x(n)={1,2,2,1} *h(n)={1,-1,-1,1}*

Write a program to compute their linear convolution using circular convolution.

8) Using a rectangular window, design a FIR low-pass filter with a pass-band gain of unity, cut off frequency of 1000 Hz and working at a sampling frequency of 5 KHz. Take the length of the impulse response as 17.

9) Design an FIR filter to meet the following specifications:
Passband edge F_p=2 KHz
Stopband edge F_s=5 KHz
Passband attenuation A_p=2 dB
Stopband attenuation A_s=42 dB
Sampling frequency F_{sf}=20 KHz

10) The frequency response of a linear phase digital differentiator is given by

1. $H_d(e^{jw}) = jwe^{-j|w|} |w| \leq \pi$

Using a Hamming window of length M = 21, design a digital FIR differentiator. Plot the amplitude response

References for laboratory work:

1) A Guide to MATLAB, B. R. Hunt, R. L. Lipsman and J. M. Rosenberg, 3rd edition, 2014, Cambridge University Press.

2) Fundamentals of Digital Signal processing using MATLAB, R. J. Schilling and S. L. Harris, 2005, Cengage Learning.

3) Getting started with MATLAB, R. Pratap, 2010, Oxford University Press.

Semiconductor Devices Fabrication

DSE (Electronics) Sem V
(For Physics and Electronics as core subjects)

		Credit distribution of the course			Eligibility Criteria	Pre-requisite of the course
		Lecture	Tutorial	Practical		
Semiconductor Devices Fabrication	4	2	0	2	Class XII pass with Physics and Mathematics as main subjects	NIL

LEARNING OBJECTIVES

This course provides a review of basics of semiconductors such as energy bands, doping, defects etc. and introduces students to various semiconductor and memory devices, thin film growth techniques and processes including various vacuum pumps, sputtering, evaporation, oxidation and VLSI processing are described in detail. By the end of the syllabus, students will have an understanding of MEMS based transducers.

LEARNING OUTCOMES

At the end of this course, students will be able to achieve the following learning outcomes.

- Learn to distinguish between single crystal, polycrystalline and amorphous materials based on their structural morphology and learn about the growth of single crystals of silicon, using Czochralski technique, on which a present day electronics and IT revolution is based.
- Students will understand about the various techniques of thin film growth and processes.
- Appreciate the various VLSI fabrication technologies and learn to design the basic fabrication process of R, C, P- N Junction diode, BJT, JFET, MESFET, MOS, NMOS, PMOS and CMOS technology.
- Gain basic knowledge on overview of MEMS (Micro-Electro-Mechanical System) and MEMS based transducers.

THEORY COMPONENT

Unit – I (9 Hours)

Introduction: Review of energy bands in materials, metal, semiconductor and insulator, doping in semiconductors, defects (point, line, Schottky and Frenkel), single crystal, polycrystalline and amorphous materials, Czochralski technique for silicon single crystal growth, silicon wafer slicing and polishing.
Vacuum Pumps: Primary pump (mechanical) and secondary pumps (diffusion, turbomolecular, cryopump, sputter-ion) – basic working principle, throughput and characteristics in reference to pump selection, vacuum gauges (Pirani and Penning)

Unit – II (10 Hours)

Thin film growth techniques and processes: Sputtering, evaporation (thermal, electron beam)pulse laser deposition (PLD), chemical vapour deposition (CVD), epitaxial growth Thermal oxidation process (dry and wet) passivation, metallization, diffusion

Unit – III (7 Hours)

VLSI Processing: Clean room classification, line width, photolithography: resolution and process, positive and negative shadow masks, photoresist, step coverage, developer, electron beam lithography, etching: wet etching, dry etching (RIE and DRIE), basic fabrication process of R, C, P-N Junction diode, BJT, JFET, MESFET, MOS, NMOS, PMOS and CMOS technology, wafer bonding, wafer cutting, wire bonding and packaging issues (qualitative idea)

Unit – IV (4 Hours)

Micro Electro-Mechanical System (MEMS): Introduction to MEMS, materials selection for MEMS devices, selection of etchants, surface and bulk micromachining, sacrificial subtractive processes, additive processes, cantilever, membranes, general idea of MEMS based pressure, force, and capacitance transducers

References:

Essential Readings:

1) Physics of Semiconductor Devices, S. M. Sze. Wiley-Interscience.
2) Fundamentals of Semiconductor Fabrication, S.M. Sze and G. S. May, John-Wiley and Sons, Inc.
3) Introduction to Semiconductor materials and Devices, M. S. Tyagi, John Wiley & Sons 4) VLSI Fabrication Principles (Si and GaAs), S. K. Gandhi, John Wiley & Sons, Inc.

Additional Readings:

1) Handbook of Thin Film Technology, L. I. Maissel and R. Glang

PRACTICAL COMPONENT

(15 Weeks with 4 hours of laboratory session per week)

At least six experiments to be performed from the following list

1. Deposition of thin films using dip coating and deposition of metal contacts using thermal Evaporation and study its I-V characteristics

2. Deposition of thin films using spin coating and deposition of metal contacts using thermal evaporation and study its I-V characteristics
3. Fabrication of p-n Junction diode and study its I-V characteristic
4. Create vacuum in a small tube (preferably of different volumes) using a mechanical rotary pump and measure pressure using vacuum gauges.
5. Selective etching of different metallic thin films using suitable etchants of different concentrations.
6. Wet chemical etching of Si for MEMS applications using different concentrations of etchant.
7. Calibrate semiconductor type temperature sensor (AD590, LM 35, LM 75)
8. To measure the resistivity of a semiconductor (Ge) crystal with temperature (up to 150C) by four-probe method.
9. To fabricate a ceramic and study its capacitance using LCR meter.
10. To fabricate a thin film capacitor using dielectric thin films and metal contacts and study its capacitance using LCR meter

References for laboratory work:

1) The science and Engineering of Microelectronics Fabrication, S. A. Champbell, 2010, Oxford University Press

2) Introduction to Semiconductor Devices, F. Kelvin Brennan, Cambridge University Press, 2010

VERILOG AND FPGA based System design

DSE (Electronics) Sem V
(For Physics and Electronics as core subjects)

Course Title & Code	Credits	Credit distribution of the course			Eligibility Criteria	Pre-requisite of the course
		Lecture	Tutorial	Practical		
Verilog and FPGA based System Design Physics DSE 14	**4**	**2**	**0**	**2**	Class XII pass with Physics and Mathematics as main subjects	Basics of digital electronics

LEARNING OBJECTIVES

This course trains the students to use VLSI design methodologies and simulate simple digital systems. Students will understand the HDL design flow and the fundamental Verilog concepts in-lieu of today's most advanced digital design techniques. The emphasis of this course is to enhance the understanding of Programmable Logic Devices so as to implement the Digital Designs on FPGAs using Verilog HDL

LEARNING OUTCOMES

At the end of this course, students will be able to,
- Write synthesizable Verilog code.
- Write a Verilog test bench to test Digital Logic Design.
- Design and simulate digital circuits using Verilog modules.
- Understand various types of programmable logic building blocks such as PAL, PLA,

CPLDs and FPGAs and their trade-offs.
- Design and implement digital systems on programmable logic device FPGA using

Verilog HDL.

THEORY COMPONENT

Unit – I (20 Hours)

Introduction to Verilog: Introduction to HDL, importance of HDL, popularity of Verilog HDL, design flow, structure of HDL module, Verilog modules (design and stimulus), introduction to language elements - keywords, identifiers, white space, comments, format, integers, real and strings, logic values, data types, scalars and vector nets, parameters, system tasks, compiler directives

Gate level modelling: Introduction, built in primitive gates, buffers, multiple input gates, gate delays.
Data flow modelling: Continuous assignment, net declaration assignments, net delays, operator types and operators precedence

Behavioral modelling: Always and initial constructs, procedural assignment (blocking and non-blocking statements), If-else, case statements, loop structures (while, for, repeat and forever), sequential and parallel Blocks
Modelling of combinational and sequential digital circuits using different levels of abstraction

Hierarchical modelling concepts: Design methodologies, design a 4-bit adder using four 1-bit full adders

Unit – II (10 Hours)

Look up Tables: 2-input, 3-input and 4-input LUTs, Implement logic functions with LUT, advantages and disadvantages of lookup tables
Programmable Logic Devices: Difference between PAL and PLA, Realize simple logic functions using PAL and PLA, CPLD and FPGA architectures, types of FPGA, logic cell structure, programmable interconnects, logic blocks and I/O Ports, placement and routing, applications of FPGAs

References:
Essential Readings:
1) Verilog HDL. Pearson Education, S. Palnitkar, 2 edition, 2003
2) FPGA Based System Design. W. Wolf, Pearson Education
3) Digital Signal processing, S. K. Mitra, 1998, McGraw Hill
4) VLSI design, D. P. Das, 2nd edition, 2015, Oxford University Press.
5) Digital Signal Processing with FPGAs, U. Meyer Baese, Springer, 2004

Additional Readings:

1) Fundamentals of Digital Logic with Verilog Design, S. B. Zvonko Vranesic, 2016, McGraw Hill

PRACTICAL COMPONENT

(15 Weeks with 4 hours of laboratory session per week)

- Session on how to write the design module and test benches using required software and simulate the combinational and sequential circuits.
- Sessions on how to configure FPGA using Verilog HDL for the final implementation of the logic design.

At least six experiments to be performed from the following list

1) Half adder, Full Adder using basic and derived gates.
2) Half subtractor and Full Subtractor using basic and derived gates.
3) Design and simulate 4-bit Adder using Data Flow Modeling.
4) Multiplexer (4x1) and Demultiplexer(1X4) using Data Flow Modeling.
5) Decoder and Encoder using case structure/gates.
6) Clocked D, JK and T Flip flops (with Reset inputs)
7) 4-bit Synchronous up/downCounter
8) To design and study switching circuits (LED blink shift)
9) To interface LCD using FPGA
10) To interface a multiplexed seven segment display.
11) To interface a stepper motor and DC motor.

References for laboratory work:

1) Digital System Designs and Practices: Using Verilog HDL and FPGAs, Ming-Bo Lin, Wiley India Pvt Ltd.

2) Verilog Digital System Design, Z. Navabi, 2nd edition, TMH
3) Designing Digital Computer Systems with Verilog, D. J. Laja and S. Sapatnekar, 2015,

Cambridge University Press nd
4) Verilog HDL primer, J. Bhasker. BSP, 2 edition, 2003