1) Half adder, Full Adder using basic and derived gates.
2) Half subtractor and Full Subtractor using basic and derived gates.
3) Design and simulate 4-bit Adder using Data Flow Modeling.
4) Multiplexer (4x1) and Demultiplexer(1X4) using Data Flow Modeling.
5) Decoder and Encoder using case structure/gates.
6) Clocked D, JK and T Flip flops (with Reset inputs)
7) 4-bit Synchronous up/downCounter
8) To design and study switching circuits (LED blink shift)
9) To interface LCD using FPGA
10) To interface a multiplexed seven segment display.
11) To interface a stepper motor and DC motor.

References for laboratory work:

1) Digital System Designs and Practices: Using Verilog HDL and FPGAs, Ming-Bo Lin, Wiley India Pvt Ltd.

2) Verilog Digital System Design, Z. Navabi, 2nd edition, TMH
3) Designing Digital Computer Systems with Verilog, D. J. Laja and S. Sapatnekar, 2015,

Cambridge University Press nd
4) Verilog HDL primer, J. Bhasker. BSP, 2 edition, 2003